University of Southern California

Department of Electrical Engineering - Electrophysics

EE 326Lx Essentials of Electrical Engineering

Lab #6

This lab uses the 555 timer IC as an astable multivibrator, a circuit with a periodic output state. The timing is controlled by RC (dis)charging circuits.

Before you begin ... Take note of the attached LM555 data sheet and the supporting course notes. You will need to understand the latter in order to complete your lab report.

Part A

1. Construct the circuit shown in Fig. 1.27 in the supporting course notes. Use $V^+ = 6$ V, $R_1 = R_2 = 10$ kΩ, and $C = 100$ nF. Observe the output at pin 3 with the oscilloscope.

2. Measure the frequency and duty cycle (percent of period with HIGH state) of the output waveform.

In your lab report ... Compare your 555 timer measurements with theory. Why is the output frequency independent of V^+? Is it possible to obtain a duty cycle less than 50%?

Part B

1. Connect a variable power supply to pin 5 (control) and vary the voltage from 3 V to 5 V. Observe the changes that occur in the output waveform, and record your results for 3 V and 5 V.

In your lab report . . . Derive the values of the LOW and HIGH output intervals as a function of $v_{control}$, then compare with your lab data. You will want to refer to Fig. 1.28 in the supplemental notes.

National Semiconductor

February 2000

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

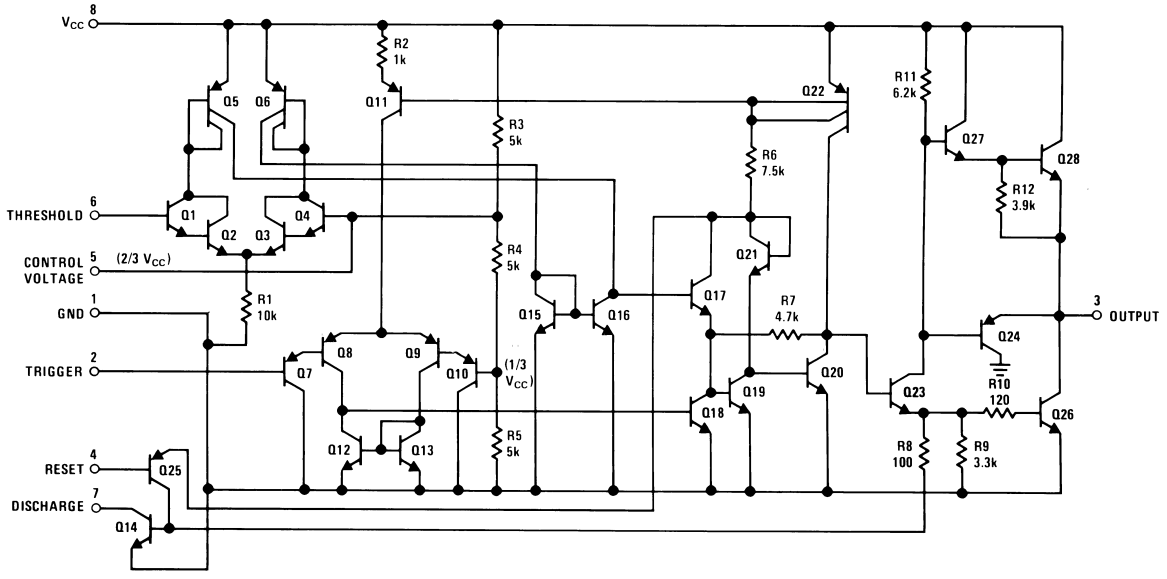
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per ˚C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



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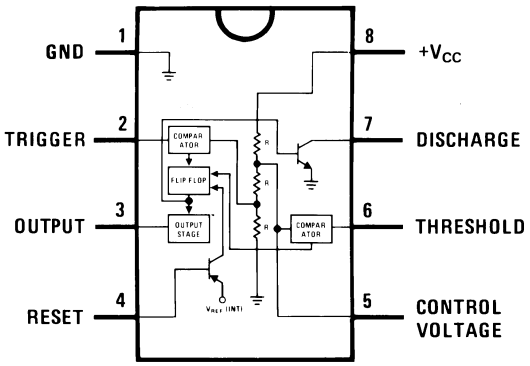
Connection Diagram

Dual-In-Line, Small Outline
and Molded Mini Small Outline Packages



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Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260˚C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215˚C
Infrared (15 Seconds)	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Electrical Characteristics (Notes 1, 2)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	6	
	V_{CC} = 15V, R_L = ∞		10	15	mA
	(Low State) (Note 4)				
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	R_A = 1k to 100kΩ,		50		ppm/˚C
	C = 0.1µF, (Note 5)				
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100kΩ,		150		ppm/˚C
	C = 0.1µF, (Note 5)				
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V		5		V
	V_{CC} = 5V		1.67		V
Trigger Current			0.5	0.9	µA
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	µA
Control Voltage Level	V_{CC} = 15V	9	10	11	V
	V_{CC} = 5V	2.6	3.33	4	
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	V_{CC} = 15V, I_7 = 15mA		180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5mA		80	200	mV

Electrical Characteristics (Notes 1, 2) (Continued)

(T_A = 25˚C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V				
	I_{SINK} = 10mA		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.75	V
	I_{SINK} = 100mA		2	2.5	V
	I_{SINK} = 200mA		2.5		V
	V_{CC} = 5V				
	I_{SINK} = 8mA				V
	I_{SINK} = 5mA		0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200mA, V_{CC} = 15V		12.5		V
	I_{SOURCE} = 100mA, V_{CC} = 15V	12.75	13.3		V
	V_{CC} = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at elevated temperatures the device must be derated above 25˚C based on a +150˚C maximum junction temperature and a thermal resistance of 106˚C/W (DIP), 170˚C/W (S0-8), and 204˚C/W (MSOP) junction to ambient.

Note 4: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 5: Tested at V_{CC} = 5V and V_{CC} = 15V.

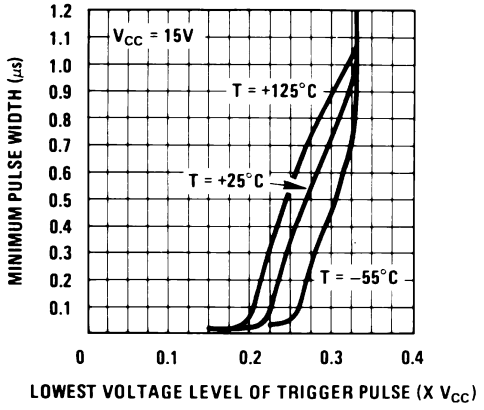
Note 6: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20MΩ.

Note 7: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 8: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Typical Performance Characteristics

Minimuim Pulse Width Required for Triggering



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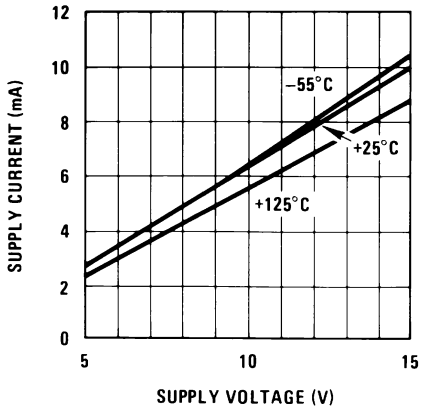
Supply Current vs. Supply Voltage



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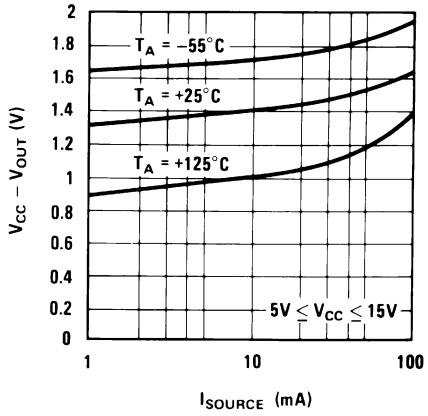
High Output Voltage vs. Output Source Current



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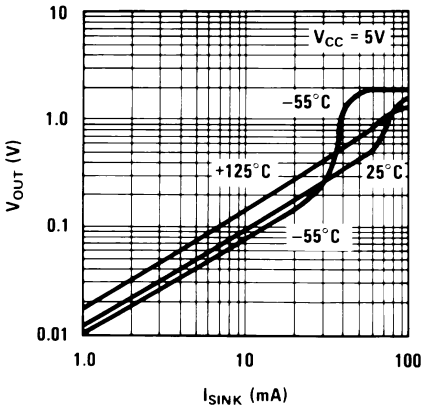
Low Output Voltage vs. Output Sink Current



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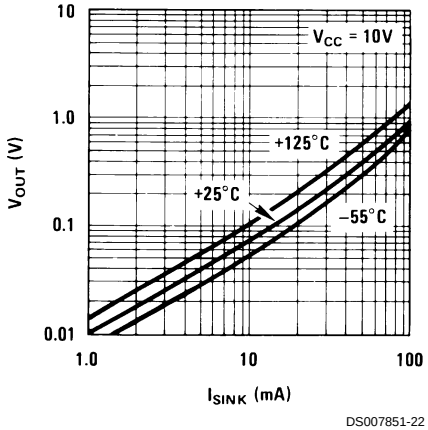
Low Output Voltage vs. Output Sink Current



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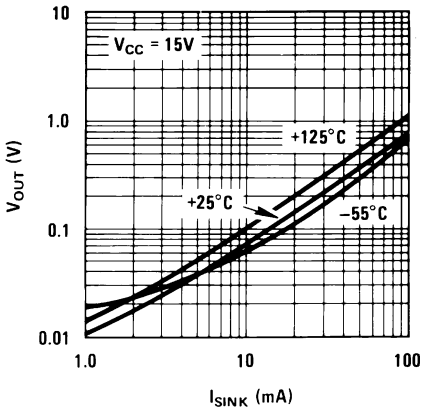
Low Output Voltage vs. Output Sink Current



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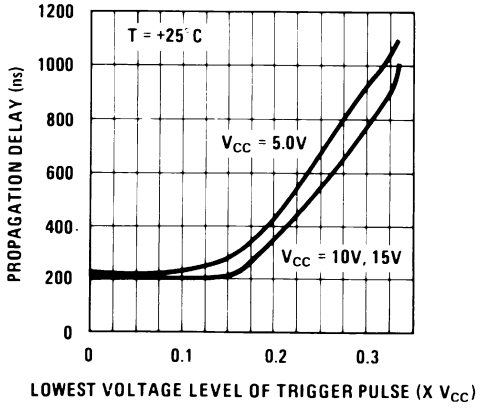
Typical Performance Characteristics (Continued)

**Output Propagation Delay vs.
Voltage Level of Trigger Pulse**



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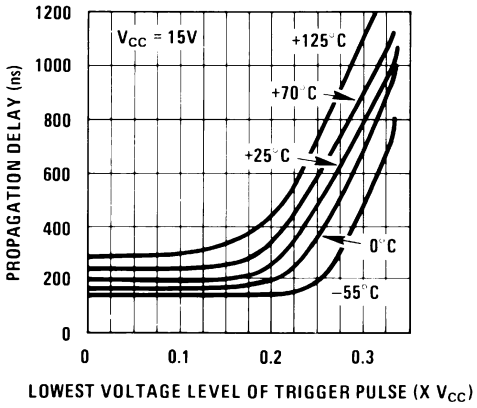
**Output Propagation Delay vs.
Voltage Level of Trigger Pulse**



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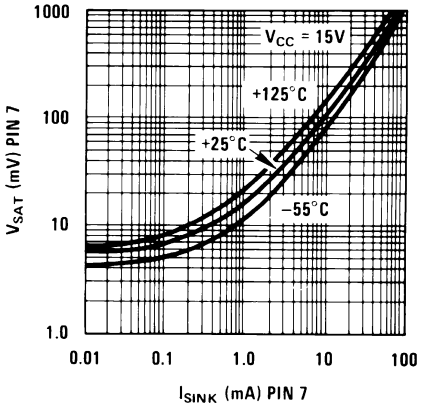
**Discharge Transistor (Pin 7)
Voltage vs. Sink Current**



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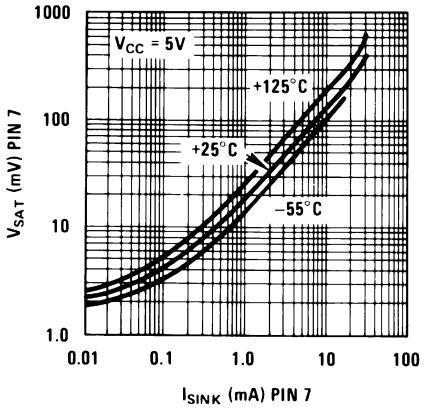
**Discharge Transistor (Pin 7)
Voltage vs. Sink Current**



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Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

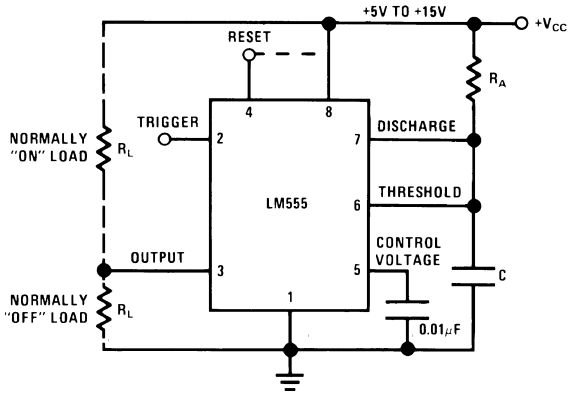
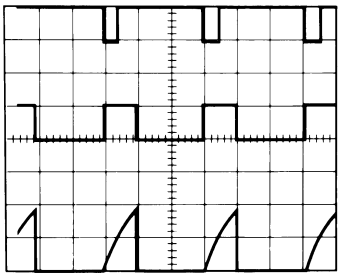


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



V_{CC} = 5V — Top Trace: Input 5V/Div.
TIME = 0.1 ms/DIV. — Middle Trace: Output 5V/Div.
R_A = 9.1kΩ — Bottom Trace: Capacitor Voltage 2V/Div.
C = 0.01μF

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least 10μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

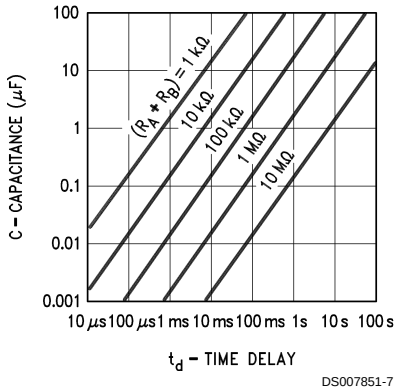


FIGURE 3. Time Delay

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

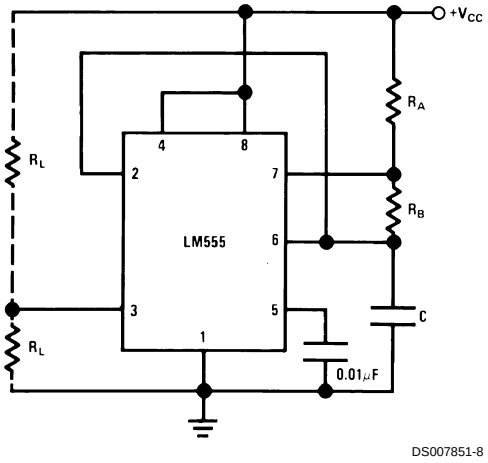
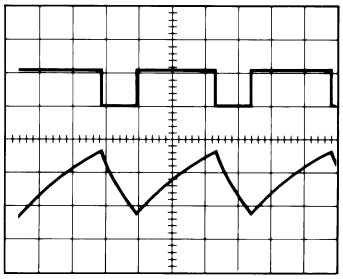


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



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V_{CC} = 5V Top Trace: Output 5V/Div.
TIME = 20µs/DIV. Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

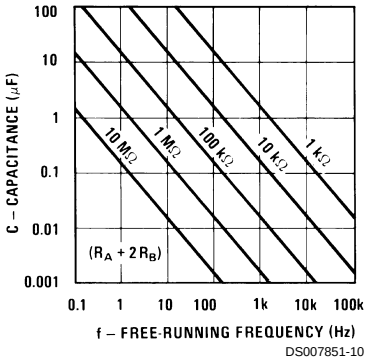

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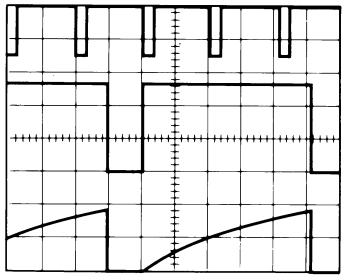
FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



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V_{CC} = 5V Top Trace: Input 4V/Div.
TIME = 20µs/DIV. Middle Trace: Output 2V/Div.
R_A = 9.1kΩ Bottom Trace: Capacitor 2V/Div.
C = 0.01µF

FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

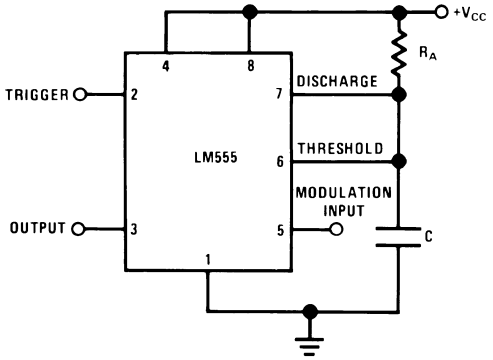

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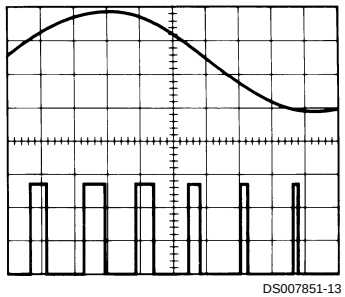
FIGURE 8. Pulse Width Modulator



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V_{CC} = 5V Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.
R_A = 9.1kΩ
C = 0.01µF

FIGURE 9. Pulse Width Modulator

Applications Information (Continued)

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

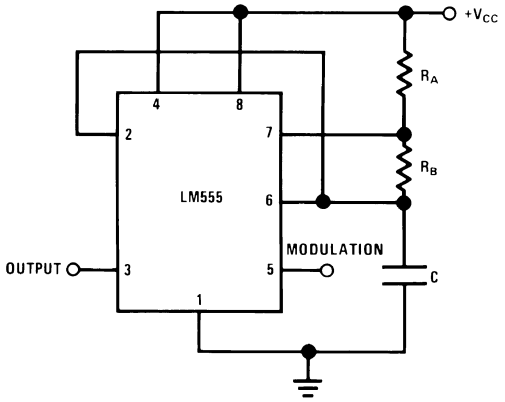
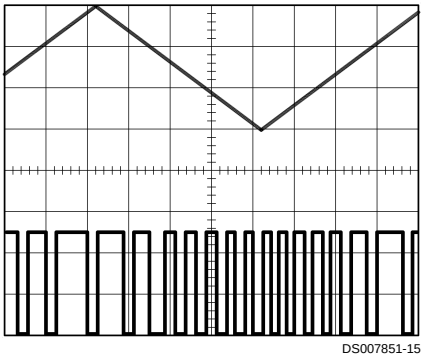


FIGURE 10. Pulse Position Modulator



V_{CC} = 5V Top Trace: Modulation Input 1V/Div.
TIME = 0.1 ms/DIV. Bottom Trace: Output 2V/Div.
R_A = 3.9kΩ
R_B = 3kΩ
C = 0.01µF

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

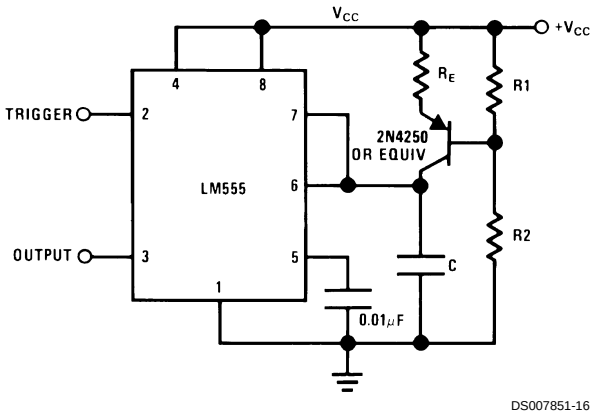


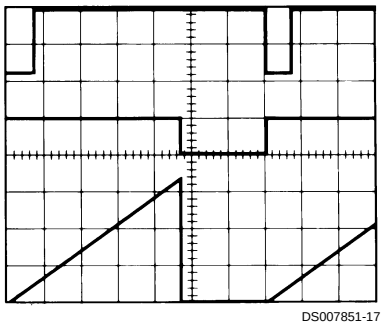
FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$

$$V_{BE} \simeq 0.6V$$



V_{CC} = 5V Top Trace: Input 3V/Div.
TIME = 20µs/DIV. Middle Trace: Output 5V/Div.
R_1 = 47kΩ Bottom Trace: Capacitor Voltage 1V/Div.
R_2 = 100kΩ
R_E = 2.7 kΩ
C = 0.01 µF

FIGURE 13. Linear Ramp

Applications Information (Continued)

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C\ \ell n \left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$

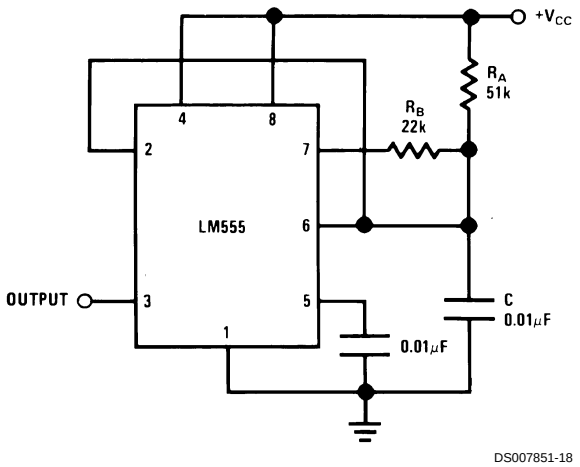


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

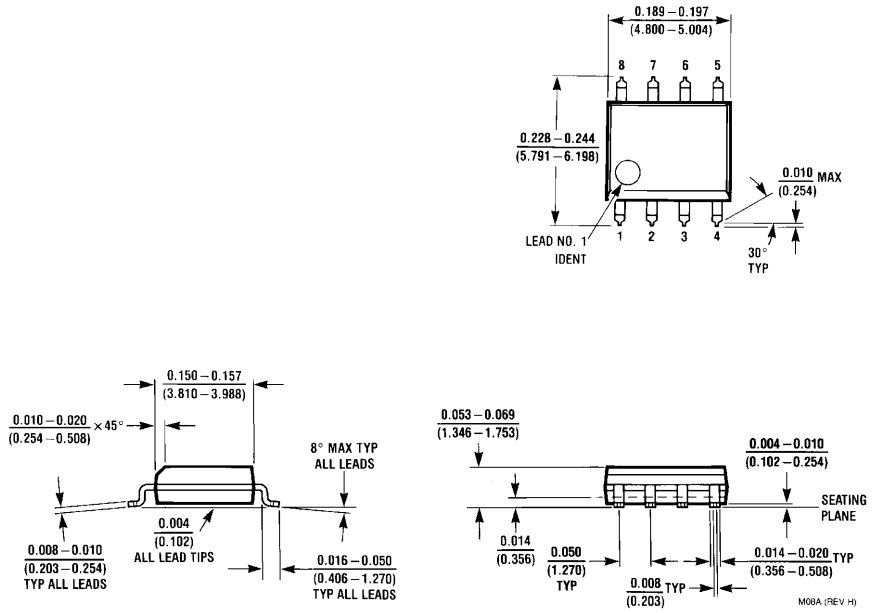
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1µF in parallel with 1µF electrolytic.

Lower comparator storage time can be as long as 10µs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10µs minimum.

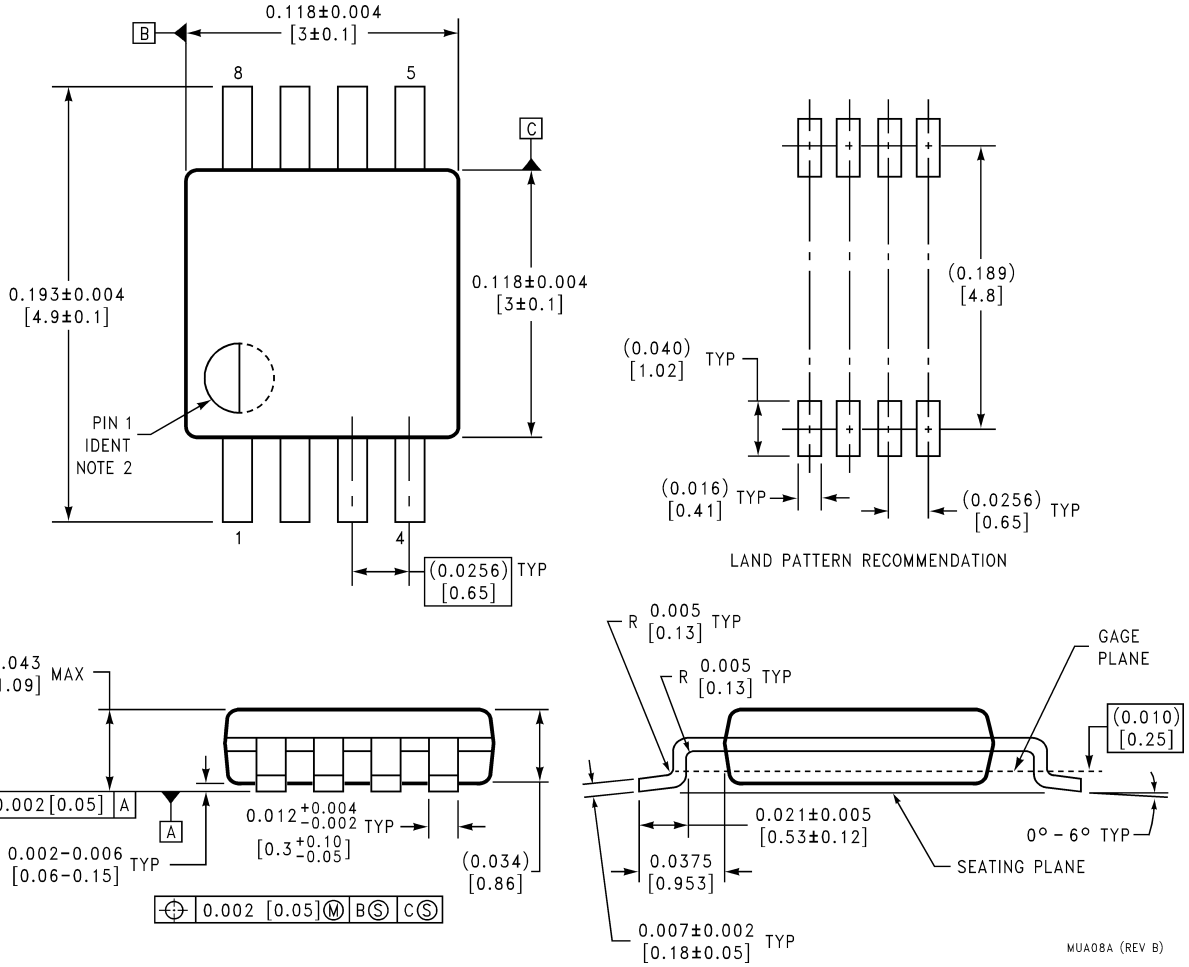
Delay time reset to output is 0.47µs typical. Minimum reset pulse width must be 0.3µs, typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

Physical Dimensions inches (millimeters) unless otherwise noted

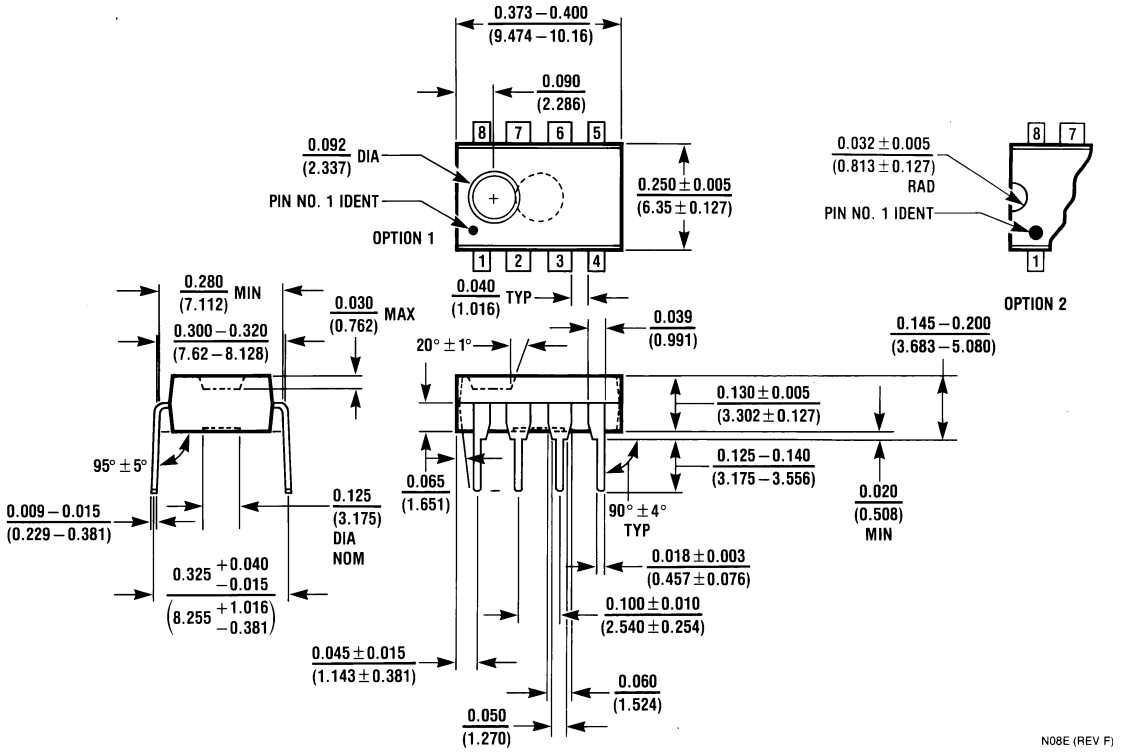


Small Outline Package (M)
NS Package Number M08A



8-Lead (0.118” Wide) Molded Mini Small Outline Package
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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1.3 Mixed Signals: The 555 Timer

We crave for more. The **555 Timer** has been around since the early 1970s. And even with the occasional new arrival of challengers offering improved performance, it remains a low-cost integrated circuit with popular appeal.

In relation to the black box shown in Fig. 1.22, the 555 timer sports ...

- Two power connections — V^+ (pin 8) and ground (pin 1).
- Two inputs — The **trigger** (pin 2) and **threshold** (pin 6) are inputs that only have effect when they are made less than or greater than specific reference voltages.
- Two outputs — The **output** (pin 3) and **discharge** (pin 7) assume one of two states: When the output is HIGH (typically $V^+ - 0.9$ V), *the discharge connection appears as an open circuit.* When the output is LOW (typically 0.2 V), *the discharge connection appears as a short circuit to ground.*
- Two special connections — The **reset** (pin 4) forces a LOW output at pin 3 when set to a LOW voltage, and it has no effect when set to a HIGH voltage. The **control** (pin 5) is used to change the values of the reference voltages that govern the behavior of the two inputs. (We shall tend to ignore both special connections.)

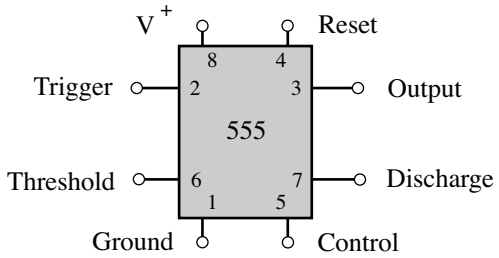

Figure 1.22: Pin designations for the 555 timer.

There are three simple governing rules:

Rule 1: Absent the condition of Rule 2, *the output goes HIGH and stays there if the trigger voltage is made less than* $(1/3)V^+$.

Rule 2: Absent the condition of Rule 1, *the output goes LOW and stays there if the threshold voltage is made greater than* $(2/3)V^+$.

Rule 3: *The input terminal currents are ideally zero.*

What do these rules provide? Suppose the initial output, trigger, and threshold voltages are LOW, 6 V, and 0 V, respectively, and let $V^+ = 6$ V. If the trigger is subsequently set to 0 V, which is less than $(1/3)V^+ = 2$ V, Rule 1 tells us that the output will become HIGH and stay there indefinitely (even as the trigger is set back to 6 V shortly afterwards). This is consistent with the output waveform time dependence shown in Fig. 1.23.

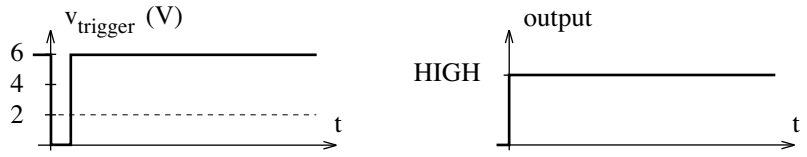

Figure 1.23: 555 trigger and output waveforms.

Nothing very exciting so far. However, we can limit the time duration of the HIGH output condition by taking advantage of Rule 2 —we merely force the *threshold* voltage to exceed $(2/3)V^+ = 4$ V at some time after the completion of the trigger pulse. One way to do this is to connect the threshold input to the RC circuit shown in Fig. 1.24a. The initial threshold voltage v_{th} is 0 V, and the threshold terminial draws no current (Rule 3). Thus, at time t,

$$v_{th} = V^+ \left(1 - e^{-t/RC}\right) . \tag{1.21}$$

In turn, $v_{th} = (2/3)V^+$ at time

$$T = RC \ln 3 = 1.1\, RC . \tag{1.22}$$

The consistent threshold and output waveforms appear in Fig. 1.24b.

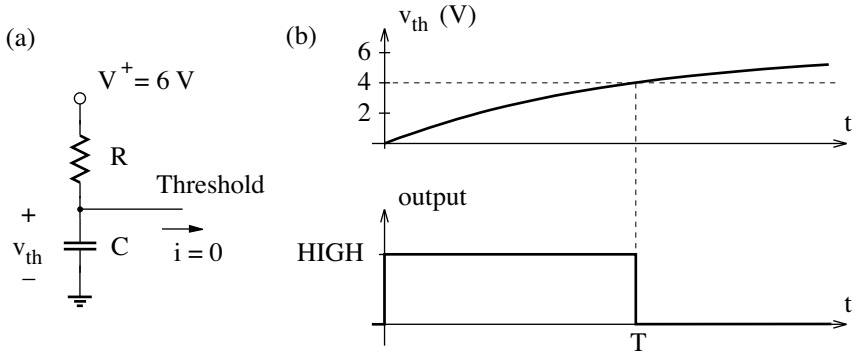

Figure 1.24: (a) 555 threshold circuit; (b) threshold and output waveforms.

Things are looking much better, apart from a minor technical difficulty: How can we ensure that the threshold voltage begins to rise when the 555 output goes HIGH? And how can we ensure that the system produces another output pulse in response to a subsequent trigger signal?

Both problems are resolved by tying the 555 discharge to the threshold input. When the output is initially LOW, the discharge appears as a short circuit to ground, and it holds the threshold to an approximate zero level. When the output becomes HIGH, the discharge appears as an open circuit, and the threshold voltage is made free to rise. When the output becomes LOW again, the discharge forces the threshold voltage back near zero.

So now we have a 555 **monostable** or **one-shot** circuit that produces a long output pulse of *fixed* duration in response to a shorter trigger pulse of *arbitrary* duration. The complete monostable circuit is shown in Fig. 1.25. Note that the reset terminal is tied to V^+, and the control terminal is tied to ground through a 0.01-μF capacitor (to suppress undesired transients).

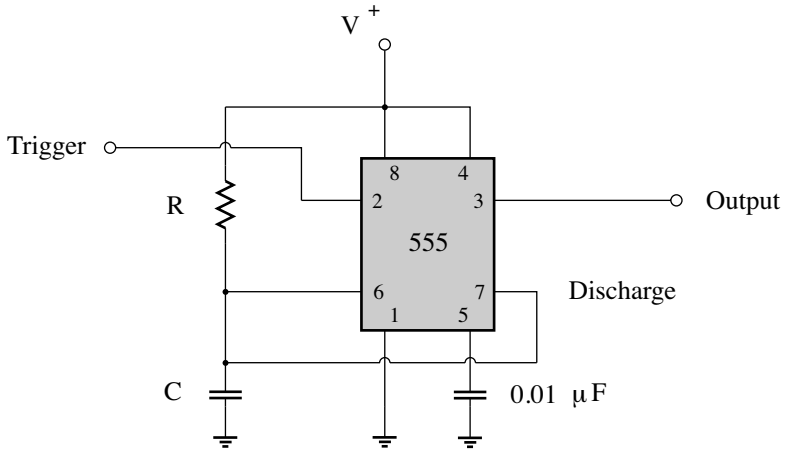

Figure 1.25: 555 monostable circuit.

Exercise 1.8 A 555 monostable circuit is intended to produce a 0.5-s output pulse subject to a design with $C = 0.1$ μF. Determine R.

Ans: $R = 4.5$ MΩ

Exercise 1.9 The capacitor of the preceding exercise discharges through an effective resistance of 1 Ω. Determine the time needed for the threshold voltage to return to 0.2 V from its highest value. Assume $V^+ = 6$ V.

Ans: $t = 0.3$ μs

Astable Behavior

Our prospects for another useful 555 circuit will soon become apparent with the help of Fig. 1.26. Here, voltage v_c is $(2/3)V^+$ when the switch is closed at $t = 0$. Our interest is the time at which $v_c = (1/3)V^+$.

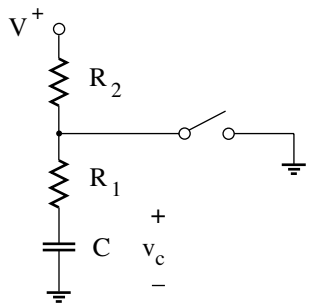

Figure 1.26: RC demonstration circuit.

The capacitor voltage decreases exponentially between initial and final values with time constant R_1C. Specifically,

$$v_c(t) = v_{final} + (v_{initial} - v_{final})\, e^{-t/R_1C} \,. \tag{1.23}$$

So with $v_{initial} = (2/3)V^+$ and $v_{final} = 0$,

$$v_c(t) = \frac{2}{3}\, V^+ \, e^{-t/R_1C} \,. \tag{1.24}$$

And when $v_c = (1/3)V^+$,

$$t = t_1 = R_1C \, \ln 2 = 0.693 \, R_1C \,. \tag{1.25}$$

Now open the switch again at $t' = t - t_1 = 0$. Our new interest is the time at which $v_c = (2/3)V^+$ —the initial condition of the preceding process. The capacitor voltage increases exponentially between $v_{initial} = (1/3)V^+$ and $v_{final} = V^+$ with time constant $(R_1 + R_2)C$. Thus, we look to the form of Eq. 1.23 to obtain

$$v_c(t') = V^+ - \frac{2}{3}\, V^+ \, e^{-t'/(R_1+R_2)C} \,. \tag{1.26}$$

In turn, when $v_c = (2/3)V^+$,

$$t' = t_2 = (R_1 + R_2)C \, \ln 2 = 0.693 \, (R_1 + R_2)C \,. \tag{1.27}$$

If the switching cycle repeats indefinitely, the frequency is

$$f = \frac{1}{t_1 + t_2} = \frac{1.443}{(2R_1 + R_2)C} \,. \tag{1.28}$$

Enter the 555 timer. In consideration of Rule 1 and Rule 2, we connect the trigger and threshold inputs to v_c so that the 555 output becomes HIGH when $v_c < (1/3)V^+$ and LOW when $v_c > (2/3)V^+$. The v_c time dependence is not affected (Rule 3). Thus, the LOW and HIGH intervals are t_1 and t_2, respectively.

While the 555 output is LOW (and v_c decreases), the discharge appears as a short circuit to ground—just like the switch. And while the 555 output is HIGH (and v_c increases), the discharge appears as an open circuit—just like the switch. So we can eliminate the switch and, more importantly, sustain the switching cycle by connecting the discharge to the node between R_1 and R_2 —another triumph for circuit feedback.

The complete 555 **astable** circuit is shown in Fig. 1.27.

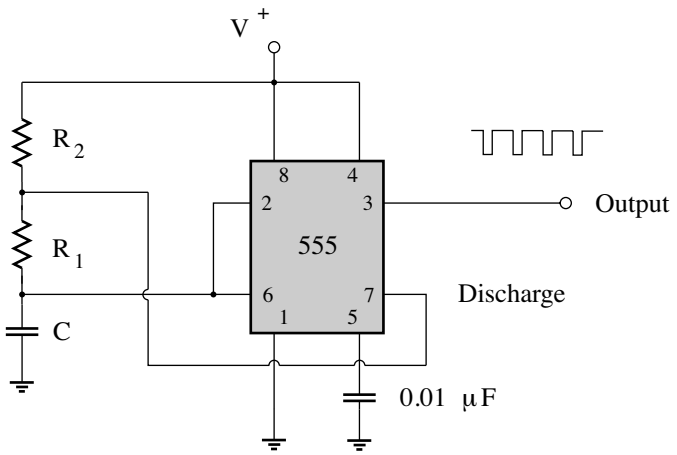

Figure 1.27: 555 astable circuit.

The **duty cycle** of the pulse train produced by a 555 astable circuit is defined as the ratio of the HIGH interval (t_2) to the waveform period ($t_1 + t_2$). Thus, in consideration of Eqs. 1.25 and 1.27,

$$\text{duty cycle} \;=\; \frac{R_1 + R_2}{2R_1 + R_2} \times 100\,\%\,. \tag{1.29}$$

If $R_1 \gg R_2$, this approaches 50 %, the duty cycle for a square-wave.

Exercise 1.10 A 555 astable circuit with the form of Fig. 1.27 is intended to produce a 2-kHz pulse train with 80% duty cycle subject to a design with $C = 0.1$ μF. Determine R_1 and R_2.

Ans: $R_1 = 1.4$ kΩ, $R_2 = 4.4$ kΩ

Inside the Black Box

Peel back the cover of a 555 timer, and you will see the assortment of interconnected components and black boxes shown in Fig. 1.28. Abstractly, you find a chain of three equal-value resistors between V^+ and ground, two op-amp-like comparators, an RS flip-flop, and an electronic device called a **transistor**—actually an npn bipolar junction transistor or BJT. No doubt you have heard of this last component, as it pervades the popular culture. For the moment, we treat the BJT as an especially fundamental black box that functions like a switch: there is an effective short circuit between the C (collector) and E (emitter) terminals when the B (base) terminal is tied through a resistor to a HIGH voltage level, and there is an open circuit between C and E when B is similarly connected to a LOW voltage level. In practice, the BJT rules are much more complicated.

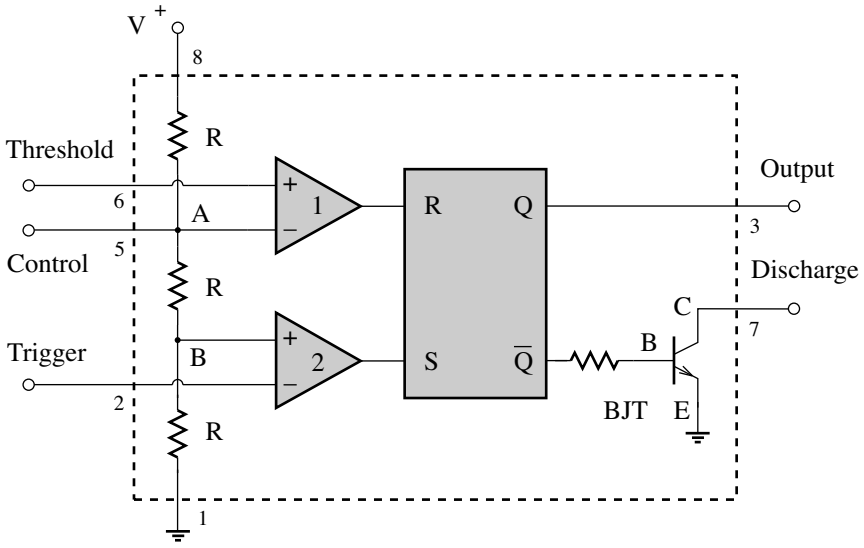

Figure 1.28: Inside the 555 timer.

The new 555 abstraction explains the output and discharge conditions encountered previously. When the external output is HIGH, the internal Q output of the RS flip-flop is also HIGH, and its complement $\bar{Q}$ is LOW, which induces the BJT to make the discharge appear as an open circuit. But when the external output is LOW, Q and $\bar{Q}$ are LOW and HIGH, respectively, and the latter induces the BJT to make the discharge appear as a short circuit to ground.

Meanwhile, the internal comparators draw zero input currents (Rule 3). The three-resistor voltage divider is thus made free to establish reference voltages of $(2/3)V^+$ at node A and $(1/3)V^+$ at node B (provided that there is an open connection at the external control terminal). Then we have ...

• **Rule 1:** Absent the condition of Rule 2 means that the threshold voltage is less than $(2/3)V^+$ so that comparator 1 yields a LOW voltage at the R input to the flip-flop. And when the trigger voltage becomes less than $(1/3)V^+$, comparator 2 yields a HIGH voltage at the S flip-flop input. In turn, Q is "set" HIGH.

• **Rule 2:** Absent the condition of Rule 1 means that the trigger voltage is greater than $(1/3)V^+$ so that comparator 2 yields a LOW voltage at the S input to the flip-flop. And when the threshold voltage becomes greater than $(2/3)V^+$, comparator 1 yields a HIGH voltage at the R flip-flop input. In turn, Q is "reset" LOW.

. . . as advertized.

Engineers design *with* integrated circuits—

only a very few actually design integrated circuits.

But woe to the engineer who overlooks the specifics of black-box interiors (see Problem 1.54).

→ Peel back the cover of an op-amp or comparator, and you will see an assortment of interconnected transistors that function much like valves—they pass current, but in an intermediate sense with not just all or nothing. How do they establish a *large* (but not infinite) differential voltage gain? What are the best input conditions that they can provide?

→ Peel back the cover of an RS flip-flop and the several covers of the gates within it, and you will see an assortment of interconnected transistors that function much like switches—shorted when closed, no current when open. How do they recognize and establish particular HIGH and LOW levels? What time constraints apply?

→ Peel back the cover of a (black-box) transistor, and you will find a device structure that is governed by a set of material and physical principles. What is the best transistor for valve- or switch-like applications?

Electronics is a discipline with an endless hierarchy of little black boxes. All of these boxes function with individual sets of ideal rules. Nevertheless, it is necessary to ask

When do the ideal black-box rules break down?

Alas, you probably skipped over the Introduction—just like most readers. So it bears repeating that this text concerns the fragility of black-box rules. Try as we may to understand electronics at the highest levels of abstraction, there's no escaping the need to peel back the covers.