

**University of Southern California**  
**Department of Electrical Engineering – Electrophysics**  
**EE 326Lx - Essentials of Electrical Engineering**  
**Course Syllabus**  
**Fall 2003**

**Abstract**

EE 326Lx serves as an introduction to the physical principles that govern the behavior of analog circuits featuring resistors, capacitors, inductors, ideal operational amplifiers, and other linear components. The primary course objective is the development of analytical techniques that simultaneously resolve current and voltage relationships within individual circuit elements and the interconnection relationships between arbitrary sets of elements (Kirchoff's current and voltage laws). Techniques range from trivial algebra with real or complex numbers to solutions of ordinary (possibly coupled) differential equations.

To be blunt, circuit analysis is dull without specific application areas of interest. In the fall semester, in which CECS majors form the majority of student constituents, the course emphasizes data conversions and data communications. In the spring semester, in which CE and ISE majors form the majority, the course emphasizes electronic instrumentation, sensors, and MEMS (micro-electromechanical systems).

EE 326Lx is a gateway course. For CECS majors, it is the foundation for VLSI systems in which non-linear circuit elements (transistors) are used in complex digital hardware such as microprocessors and high-density memory. For CE, ISE, (and CECS) majors, it is the foundation for analog electronics design (EE 348, EE 448, EE 479, etc.).

EE 326Lx is not available for credit to electrical engineering majors (who take EE 202L).

**Course Administration**

The prerequisites for EE 326Lx are PHYS 152L (Fundamentals of Physics II: Electricity and Magnetism) and MATH 126 (Calculus II). The course features a two-hour "studio" format on Wednesdays and Fridays where lecture, discussion, computer, and laboratory activities are combined in the same setting. The two-hour Monday class is generally reserved for comprehensive laboratory work. All classes meet in OHE 230.

EE 326Lx has two sections in Fall 2003:

Section1	MWF 10:00 – 11:50	(E. Maby)
Section 2	MWF 1:00 – 2:50	(V. Ng)

Students who have registered for a particular section must remain in that section.

The last day to drop the class without a W grade is 12 September, and the last day to drop the class with a W grade is 14 November. Incomplete grades (IN) are rarely assigned. The IN grade may be justified only in exceptional cases such as student illness or a personally tragic event occurring after the twelfth week of the semester.

The EE 326Lx course grade is based on the following components:

First Midterm	(6 October)	20%
Second Midterm	(10 November)	20%
Circuit Boot Camp		10%
Homework (after Boot Camp)		5%
Laboratory Reports (8)		10%
Comprehensive Design Project		5%
Final Exam		30%

Historically, the average grade for EE 326Lx is B- following the application of a “curve.” Notwithstanding, the instructors are prepared to accept a higher average if the class does exceptionally well --- for example, a class average total score of 99/100 is clearly an A.

Apart from numerical grades for the comprehensive design project and the final exam, all other grades will be posted by 14 November. It is the student’s responsibility to verify (and possibly contest) all grades **before** the final exam. **Once assigned, a letter grade will not be changed except for grossly erroneous circumstances.**

**Try not to miss class!** Students who are regularly absent invariably receive poor grades. The instructors have no reservations about compiling homework assignments and exams that are predicated, in part, on material discussed in class but not addressed in assigned textbooks or readings.

**Make-up exams (midterms or final) are not available.** If you are absent during an examination, you will receive a grade of zero unless you have a valid reason for your absence, **and you have discussed it with the instructor prior to the exam.** In the event of an excuse from a midterm, a weighted final exam score will replace the missing score. If you cheat during an exam, you will receive a grade of F in the course and you will be reported to the Office of Student Conduct for further disciplinary action.

Students are expected to complete eight Monday laboratory assignments (unless excused for illness or some compelling emergency). **If you choose not to complete all eight lab assignments, you will receive a grade of F for the course.**

The comprehensive design project will be assigned on 24 November, and a related report will be due on the last class of the semester (5 December). **If you choose not to complete the project, you will receive a zero grade for it.**

Students are encouraged to work in teams of two on labs and the final design project. Each team member will receive the same numerical grade. Collaboration on in-class exercises is especially encouraged.

Homework is crucial in EE 326Lx, since it provides much needed practice in analytical techniques, it is a good measure of whether you understand fundamental concepts, and it is a prerequisite for good performance on course exams. If your weighted course average places you on the borderline between two letter grades, a poor homework average will significantly increase the probability of the lower grade.

Much of the homework grade is weighted towards “circuit boot camp,” a collection of 30 valuable (albeit unexciting) exercises that are intended to develop circuit analysis skills. The problems will be assigned in three parts with the following due dates:

- Part 1 – 3 September
- Part 2 – 10 September
- Part 3 – 17 September

You are encouraged to use computer analysis tools such as PSpice to check homework. Be sure not to use the computer as a “crutch.” You will not have access during exams.

### **Textbook**

*Introductory Circuits for Electrical and Computer Engineering*, by James W. Nilsson and Susan A. Riedel.

### **Instructor Information:**

#### Section 1:

Edward Maby PHE 626 0-4706 [maby@usc.edu](mailto:maby@usc.edu)  
Office hours: WF 1:00 – 1:50

Brian Amanatullah [amanatul@usc.edu](mailto:amanatul@usc.edu)  
Chris Morgan [christjm@usc.edu](mailto:christjm@usc.edu)

#### Section 2:

Vincent Ng (Off Campus) (949) 753-7800 x128 [vincentn@usc.edu](mailto:vincentn@usc.edu)  
Office hours: WF 12:00 – 1:00 (PHE 624)

Brent Nash [bnash@usc.edu](mailto:bnash@usc.edu)  
Eric Webb [etw@usc.edu](mailto:etw@usc.edu)

The EE 326Lx web site is: <http://www-classes.usc.edu/engr/ee-ep/326>.

## Tentative EE 326Lx Schedule

Fall 2003

### Week 1

M	25 August	Current, voltage, power, KCL, KVL, dc circuit elements N & R: Chapter 1
W	27 August	Series and parallel R, voltage and current dividers, PSpice N & R: 2.1 – 2.2, PSpice handout
F	29 August analysis	Source transformations, superposition, node-voltage N & R: 2.3 – 2.4, 3.1 – 3.2

### Week 2

M	1 September	Labor Day
W	3 September	Mesh-current analysis, node and mesh practice problems N & R: 3.3 – 3.8
F	5 September	Thevenin and Norton equivalent circuits N & R: 3.9 – 3.11

### Week 3

M	8 September	Lab #1 – dc measurements
W	10 September	Comparators, Schmitt trigger (hysteresis) N & R: 4.7, comparator handout
F	12 September	Flash ADC (offset + gain errors, INL, DNL), thermometer code, algorithmic ADCs <a href="http://www.maxim-ic.com/appnotes.cfm/appnote_number/748">http://www.maxim-ic.com/appnotes.cfm/appnote_number/748</a>

### Week 4

M	15 September	Lab #2 – 3-bit flash ADC
W	17 September	Ideal op-amp circuits N & R: 4.1 – 4.5
F	19 September	Instrumentation amplifiers, non-ideal op-amps N & R: 4.6

**Week 5**

M	22 September	Lab #3 – ADC (IC interface and control)
W	24 September	Current-to-voltage converter, R-2R DACs DAC handout
F	26 September	LabView programming (pattern generator) LabView handouts

**Week 6**

M	29 September	Lab #4 – DAC (IC interface and control)
W	1 October	Inductance, capacitance, charge-mode ADCs and DACs N & R: 5.1 – 5.3
F	3 October	Review

**Week 7**

M	6 October	Midterm #1
W	8 October	First-order RL circuits N & R: 5.4 (pp. 198-208)
F	10 October	First-order RC circuits, integrating ADC N & R: 5.4 (pp. 208-238)

**Week 8**

M	13 October	Lab #5 – Timing circuits
W	15 October	Complex transients N & R: 6.1 – 6.2
F	17 October	Series and parallel RLC circuits N & R: 6.3 – 6.4

**Week 9**

M	20 October	Lab #6 - Resonance
W	22 October	Transmission lines, cable models Transmission-line handout #1
F	24 October	Transmission-line termination effects Transmission-line handout #2

**Week 10**

M	27 October	Lab #7 – Transmission lines
W	29 October	Phasor analysis N & R: 7.1 – 7.4
F	31 October	ac power N & R: 7.9 – 7.11

**Week 11**

M	3 November	Lab #8 - Filters
W	5 November 1	Transformers, complex impedance matching Class notes
F	7 November	Review

**Week 12**

M	10 November	Midterm #2
W	12 November	Line drivers and receivers Class notes
F	15 November	RS232, RS485, and other protocols Class notes

**Week 13**

M	17 November	Lab Make-up
W	19 November	Fiber communications, phase-locked loops Class notes
F	21 November	Wireless communications Class notes

**Week 14**

M	24 November	Project Assigned
W	26 November	no class
F	28 November	(Thanksgiving)

**Week 15**

M	1 December	Project
W	3 December	Project
F	5 December	Project Report Due