UNIVERSITY OF SOUTHERN CALIFORNIA

SCHOOL OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING-ELECTROPHYSICS

EE 348: FINAL EXAMINATION **SPRING, 1998**
(05/07/98, 4:30 -to- 6:20 PM: Open Book & Open Notes) **CHOMA**

PROBLEM #1: *(40%)*

The CMOS circuit shown in Fig. (E1) is a so called *push–pull, class B circuit*, which is commonly used as an output stage in amplifiers. The voltage, V_B, along with the static component of the input voltage, V_I, biases transistors *M3* and *M4* in their saturated domains. But the circuit is designed so that when the indicated voltage, V_A, which results from the applied input voltage, V_I, is sufficiently positive, transistor *M1* conducts, while *M2* remains cut off. On the other hand, when V_A is sufficiently negative, transistor *M2* conducts, while *M1* is cut off. Thus, for sufficiently positive V_A, transistor *M1* sources current to the load resistance, R_L, and for sufficiently negative V_A, *M2* sinks current from the load. Although substrate biasing is not shown, assume that all transistor substrates are strongly back biased and that substrate effects on threshold voltages are negligible. In the following calculations, neglect internal device source and drain resistances, and assume that the channel resistance is infinitely large. Assume further that all p–channel devices are matched and have transconductance coefficient, K_p, threshold voltage V_{hp}, and gate aspect ratio W_2/L_2. Similarly, assume all n–channel devices are matched and have transconductance coefficient, K_n, threshold voltage V_{hn}, and gate aspect ratio W_1/L_1.

(a). In terms of the power supply voltages, V_{DD} and V_{SS}, the indicated voltage, V_A, and the device threshold voltages, V_{hp} and V_{hn}, give the conditions that ensure transistor *M1* and *M2* operation in their saturated domains when they respectively conduct.

(b). When transistor *M1* conducts, derive an expression that relates the output voltage, V_O, to the voltage, V_A, for the case of small V_O.

(c). When transistor *M2* conducts, derive an expression that relates the output voltage, V_O, to the voltage, V_A, for the case of small V_O.

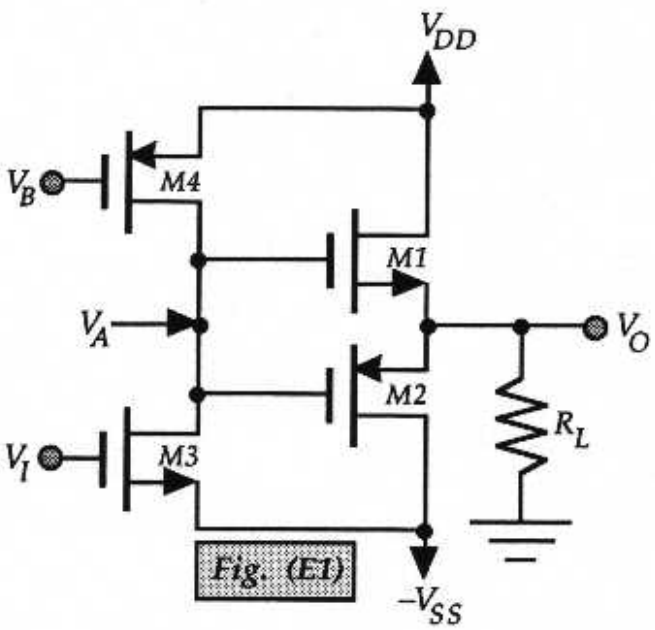

Fig. (E1)

(d). Would you advocate very large or very small gate aspect ratios if, when respective transistors conduct, the design requirements call for a nominal linear dependence of V_O on V_A and an output voltage function that is nominally independent of K_n, K_p, and R_L?

(e). Sketch V_O as a function of V_A for both negative and positive values of V_A. What problem do you see with respect to using this circuit in electronic systems having demanding linearity requirements?

PROBLEM #2: (30%)

All transistors in the bipolar differential amplifier depicted in Fig. (E2) are identical, have very large forward betas, negligible internal emitter and collector resistances, and infinitely large Early resistances. When biased properly, each transistor displays a forward base–emitter junction voltage of V_{BE}.

(a). In terms of V_{BE} and circuit parameters, find expressions for the quiescent collector currents flowing in **all** transistors and the quiescent voltages, with respect to ground, at the collectors of **all** transistors. The signal source voltage, V_s, has zero static component.

(b). Under small signal operating conditions, find the Thévenin voltage and Thévenin resistance seen looking back to the collector of transistor *Q2*. Do balanced conditions prevail under these Thévenin computational circumstances?

(c). Assuming that balanced conditions prevail in the input differential pair, find the common mode and differential mode input resistances with respect to the bases of transistors *Q1* and *Q2*.

(d). Using the results of Part (b), determine an expression for the overall voltage gain, $A_v = V_{os}/V_s$.

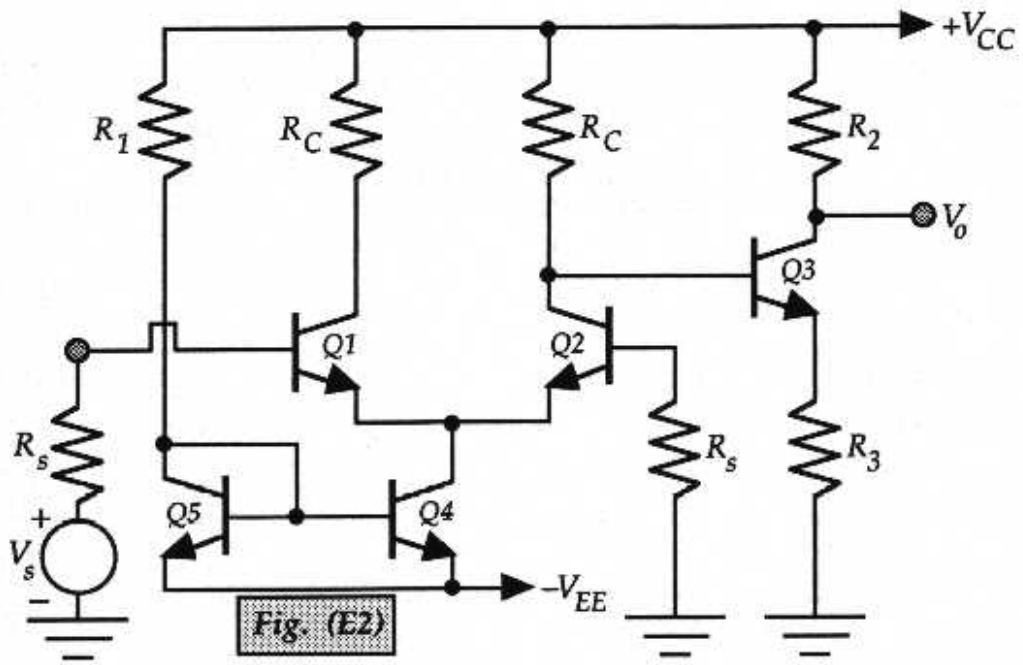

Fig. (E2)

PROBLEM #3: (30%)

The CMOS amplifier shown in Fig. (E3) is commonly used as the second stage of simple two stage operational amplifiers. The voltage, V_B, is a static source used only for biasing purposes, while I_s, is a small signal current source. All p-channel transistors have their substrate terminals connected to the V_{DD} bus, and all n-channel transistors return their substrate terminals to the $-V_{SS}$ bus. For purposes of this problem, all internal device drain and source resistances can be neglected and except for transistor *M1*, all drain–source channel resistances (r_o) can be presumed infinitely large. Thus **do not** neglect r_o in *M1*. Finally, **do not** ignore substrate transconductance effects in any transistor, and **do not** assume that the forward transconductances of all devices are identical.

(a). Derive an expression for the small signal, low frequency, forward transresistance, $Z_f = V_{os}/I_s$, of the amplifier. Approximate your expression for the case of large drain-source channel resistance in *M1*.

(b). Derive an expression for the small signal, low frequency, input resistance, R_{in}. Approximate your expression for the case of large circuit resistance, R.

(c). Derive an expression for the small signal, low frequency, output resistance, R_{out}.

(d). Using the approximate results deduced in the preceding three parts of this problem, explain the general effect on forward transresistance, input resistance, and output resistance of increasing the biasing voltage, V_B.

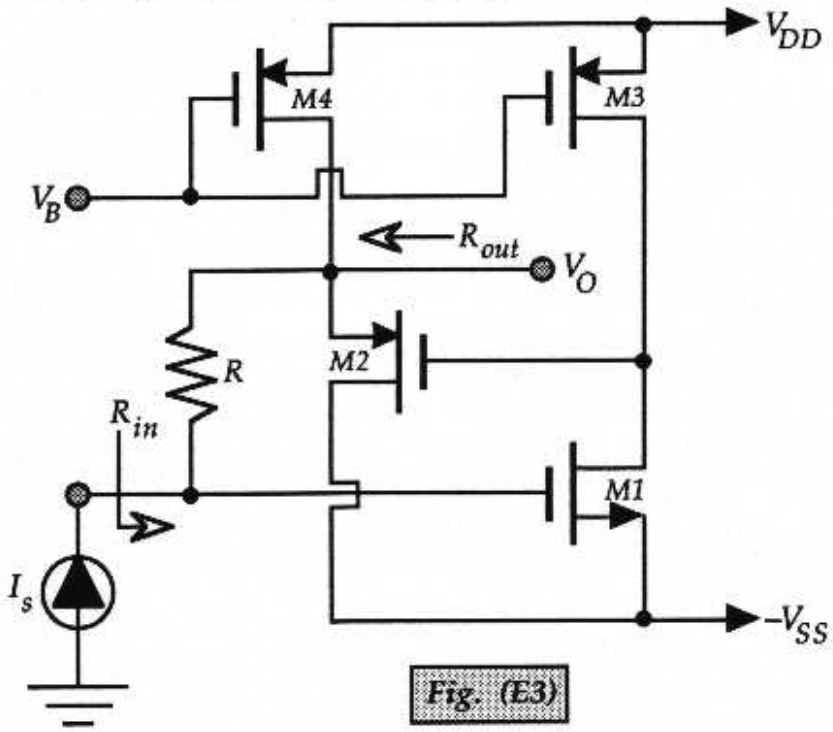

Fig. (E3)

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J. Choma, Jr., 07 May 1998