Active-low enable inputs in TTL circuits

How pull-up is possible in TTL circuits?

Consider a typical TTL OR gate (DM74LS32). From data sheet of DM74LS32, its input parameters are

\[ I_{IH} = 20 \mu A \quad I_{IL} = -0.36 \text{mA} \]
\[ V_{IH} = 2 \text{V min.} \quad V_{IL} = 0.8 \text{V max.} \]

Now consider a typical TTL tri-state buffer (DM74LS125A). From data sheet of DM74LS125A, its output parameters are

\[ I_{OH} = -2.6 \text{mA} \quad I_{OL} = 24 \text{mA} \]
\[ V_{OH} = 3.4 \text{V typ.} \quad V_{OL} = 0.35 \text{V typ.} \]
\[ I_{OZH} = 20 \mu A \quad I_{OZL} = -20 \mu A \]

Let's look at the following arrangement where four 32-bit wide, byte addressable processors access a global memory arranged in four byte-wide banks. Each bank is activated for writing by asserting its low-active write-enable input ($\overline{WE}$0.....$\overline{WE}$3). Consider the following two cases:

**No processor is accessing the bus:** When no processor is accessing memory, all $\overline{AEN}$ signals ($\overline{AEN}_A$...$\overline{AEN}_D$) are at logic 1. This disables all tri-state buffers. In this case 10K pull-up resistor pulls the $\overline{WR}_{\text{Global}}$ pin to logic 1. Now the total current which flows through 10K resistor towards tri-state buffers and OR gates is

\[ I = 4 \times I_{OZH} + 4 \times I_{IH} = 4 \times 20 \mu A + 4 \times 20 \mu A = 160 \mu A \]
Voltage \( V_a \) (at node a) = \( 5 - 160uA \times 10K = 3.4 \) volts

Above calculations show that \( V_a \) is greater than minimum \( V_{IH} \) requirement of 2 volts for 74LS32 gates. Thus \( \overline{WR} \)-Global input of all OR gates will be successfully driven high. This will disable all write enables (\( WE_0 \)....\( WE_3 \)) which are active low.

**One of the processors is accessing the bus:** Let's suppose processor A is accessing global memory for writing by activating \( \overline{AEN}_A \) and asserting \( WR_A \). Assuming a typical value of \( V_{OL} = 0.35 \) volts for tri-state buffer, voltage \( V_a \) at node a is 0.35 volts. In this case each OR gate poses a load of 360uA and three tri-state buffers, which are inactive, pose a total load of 3 \( \times I_{OZL} \). Thus the tri-state buffer, which is active, has to sink a total current:

\[
I = [4 \times 360uA] + [3 \times 20uA] + [(5 - 0.35) / 10K] = 1.965mA
\]

DM74LS125A can easily sink 24mA. Therefore it will easily drive \( \overline{WR}_{Global} \) of all OR gates to logic 0.

Above two cases show that we can easily pull up the inputs of OR gates (74LS32) using a pull up resistor.

**Why pull-down is not possible in TTL circuits?**

Once again consider the same arrangement in which four processors access a global memory but this time

\[
\begin{align*}
&\text{WR} & &\text{AEN} & &\text{BEN} & &\text{WE} & &\text{Bank} \\
&A & &A & &B & &1 & &0 \\
&B & &B & &C & &2 & &1 \\
&C & &C & &D & &3 & &2 \\
&D & &D & & & &4 & &3
\end{align*}
\]

\( WR_{Global} \) signal from processors as well as \( WE \) inputs to global memory are active high. Consider a typical NAND gate (DM74LS00). From data sheet of DM74LS00, its *input parameters* are

\[
\begin{align*}
I_{IH} &= 20uA & I_{IL} &= -0.36mA \\
V_{IH} &= 2V \text{ min.} & V_{IL} &= 0.8V \text{ max.}
\end{align*}
\]

**No processor is accessing the bus:** When all the \( \overline{AEN} \) signals (\( \overline{AEN}_A \)....\( \overline{AEN}_D \)) from microprocessors are inactive, the current which flows from tri-state buffers and NAND gates to ground is:
\[ I = 4 \times I_{OZL} + 4 \times I_{IL} = 4 \times 20\mu A + 4 \times 360\mu A = 1.52mA \]

In this case voltage \( V_a \) at node a is:

\[ V_a = 500 \text{ ohm} \times 1.52mA = .76V \]

Because \( V_a \) is less than \( V_{IL} \) requirement of NAND gates (which is 0.8V maximum), the pull-down resistor of 500 ohms has successfully driven the inputs of NAND gates to logic 0. Please note that increasing the value of 500 ohm resistor will increase voltage at node a and pull-down resistor will no longer be able to drive inputs of NAND gates to logic 0.

**One of the processors is accessing the bus:** Now consider the case when processor B wants to write to global memory. It drives \( WR_B \) to logic 1 (and \( AEN_B \) to logic 0). According to \( V_{IH} \) requirement of DM74LS00 (NAND gate), its inputs must be subjected to a minimum voltage of 2 volts when driving them to logic 1. This means voltage \( V_a \) at node a must be at least 2 volts. Thus tri-state buffer (DM74LS125A) in processor B will have to source a total current:

\[ I = 3 \times I_{OZH} + 4 \times I_{IH} + \frac{(V_a - 0)}{500} = 3 \times 20\mu A + 4 \times 20\mu A + 2 / 500 = 4.14mA \]

But DM74LS125A can only source a maximum of 2.6mA. Therefore it will not be able to drive inputs of NAND gates to logic 1. The low resistance value of the pull-down resistor became a big burden to the driving gate (DM74LS125A) as it (the pull-down resistance) consumes 4mA by itself. One may argue that we can increase the value of 500 ohm resistor to reduce burden on tri-state buffer. But increasing the value of 500 ohm resistor would not allow tri-state buffer to drive inputs of the NAND gates to logic 0 when all processors are NOT accessing the global memory.

**Conclusion**

Above discussion shows that it is not feasible to have a pull-down resistance to keep an active-high signal such as \( WR_{\text{global}} \) signal inactive when it is floating. Hence all control signals (which can float at times) are chosen to be active-low so that a pull-up resistor can keep them at inactive value when no processor is driving them.

This conclusion is true for **TTL** circuits only. You can have both pull-up and pull-down resistors in **CMOS** circuits as the input/output current parameters for **high** input/output are **NOT** that different from the input/output current parameters for **low** input/output in the case of CMOS gates.