WELCOME TO EE457

COMPUTER SYSTEMS
ORGANIZATION
THREE MAIN TOPICS

1. **CPU DESIGN**
2. **MEMORY SYSTEM**
3. **COMPUTER ARITHMETIC (simple ALU)**
4. **Advanced CPU design topics**
CPU DESIGN

MICRO-ARCHITECTURE DESIGN

GENERAL DIGITAL SYSTEM DESIGN
MEMORY SYSTEM DESIGN

CACHE

+ 

VIRTUAL MEMORY
COMPUTER ARITHMETIC

2’s Complement Arithmetic Review
Simple ALU design
FAST ADDERS (CLA)
FAST MULTIPLIERS
NON-LINEAR PIPELINES
FOR ARITHMETIC OPERATIONS
COURSE PRE-REQUISITES

EE354L (Previously called EE254L/201L)
INTRODUCTION TO DIGITAL CIRCUITS

Knowledge of some assembly language
USC undergraduates have learnt picoblaze ASM
LECTURES & DISCUSSIONS

LECTURES:
(a) 2:00-3:50PM MW OHE230
(b) 4:30-6:20PM TTh OHE136

DISCUSSIONS:
(a) 12:00-12:50PM F OHE122
(b) 2:00-2:50PM F CPA102
<table>
<thead>
<tr>
<th>Spring2022</th>
<th>EE457</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quiz</td>
<td>Fri 5:00 -8:00 PM</td>
</tr>
<tr>
<td>MT</td>
<td>Fri 5:00 -8:00 PM</td>
</tr>
<tr>
<td>Final</td>
<td>Wed 3:30 -6:30 PM</td>
</tr>
</tbody>
</table>

**Quiz (~11%)**: Friday, Feb. 11, 2022, 05:00 PM – 08:00 PM PST

**Midterm (~23.5%)**: Friday, Mar. 25, 2022, 05:00 PM – 08:00 PM PST

**Final Exam (~33.5%)**: Wednesday, May 11, 2022, 03:30 PM – 06:30 PM PST
## COURSE WEIGHTS
(extract from your syllabus)

### d) Grading Policy:

<table>
<thead>
<tr>
<th>Course weights</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Assignments</strong></td>
<td>percentage</td>
<td>Late submission penalty for assignments</td>
</tr>
<tr>
<td><strong>Homeworks</strong> (short and long) (Individual work)</td>
<td>about 8% to 9%</td>
<td>5% penalty per day for long homeworks up to 3 days if solution is not given out. For short homeworks, solution is given away at the time of the assignment. 5% penalty per day up to 3 days for short homeworks also.</td>
</tr>
<tr>
<td><strong>Labs (Teamwork)</strong></td>
<td>about 23% to 24%</td>
<td>3% flat penalty up to 3 days</td>
</tr>
<tr>
<td><strong>Exams</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiz</td>
<td>Scale1</td>
<td>Scale2</td>
</tr>
<tr>
<td>Midterm</td>
<td>21%</td>
<td>26%</td>
</tr>
<tr>
<td>Final</td>
<td>37%</td>
<td>30%</td>
</tr>
</tbody>
</table>

**Attendance** is noted based on in-person attendance.
Zoom meeting participation is for students registered in the [30595D DEN@Viterbi section](#)

**Penalty** for lecture absence: 1% of the course for the 4th and the 5th; 2% for the 6th and thereafter

**Penalty** for discussion absence: 0.5% for the 4th and the 5th; 1% for the 6th and thereafter
LATE PENALTY

Long Homeworks:

Up to 5% per day for one day only if solution is not distributed

Short Homeworks:

5% per day for one day only

Solution is given away for some of them at the time of assignment.
LATE PENALTY

LABS:

3% flat penalty for 3 days late
LECTURE CLASS ATTENDANCE
(We note your attendance through Zoom meeting participation lists)

PENALTY FOR MISSING:
1% FOR 4th AND 5TH
2% FOR 6TH AND AFTER

PENALTY FOR MISSING DISCUSSION CLASS:
HALF OF LECTURE CLASS MISSING PENALTY
0.5% FOR 4th AND 5TH
1% FOR 6TH AND AFTER
DEN REMOTE STUDENTS

It is **not necessary** for you to watch lectures/discussions **synchronously**. Please send an **email** informing the three Mentors and me that you watched the week’s lectures and discussion before Monday of the next week.

gandhi@usc.edu

EE457 Mentor -- Zhijun Gui <zgui@usc.edu>,
EE457 Mentor -- Srikanth Gadde <sgadde@usc.edu>,
EE457 Mentor -- Ayush Singh <ayushs@usc.edu>
DESIGN PROJECTS

PARTIALLY COMPLETE DESIGN FILES
Core design Verilog file:
~70% complete
Testbench and wave.do files:
100% complete
You use Modelsim (or Questasim) to simulate your HDL designs.

TTL DATABOOK → NOT NECESSARY
Esperan Verilog Reference Guide

Is posted on the BB for personal use of USC faculty and students. Please do not distribute or post anywhere.
HOMEWORKs (Long and Short):
(paper (scanned pdf) submission on D2L)

INDIVIDUAL EFFORT

LAB:

(1) VERILOG CODING,
SIMULATION AND DEBUGGING
(online Unix Submission on
viterbi-scf1.usc.edu or viterbi-scf1.usc.edu)

TEAM EFFORT

(2) JUSTIFICATION,
END-OF-LAB QUESTIONS
(paper (scanned pdf) submission on D2L)

INDIVIDUAL EFFORT
CLASS WEBPAGE
DEN D2L (Desire 2 Learn)
https://courses.uscden.net/d2l/login

EE457Lx - 20221 - Computer Systems Organization
Spring 2022
USC Viterbi School of Engineering – DEN@Viterbi

Log in to view your courses offered through DEN@Viterbi, explore tools and features, and customize your eLearning experience for programs and courses supported by DEN@Viterbi. Students must be registered and approved to view select courses.

First Time Logging in?

DEN@Viterbi Students: You must create a profile first before you can log in. Create a profile

On-campus students: Profile is created automatically.

If you have problems logging on or seeing your courses, please contact DEN@Viterbi Technical Support Center office at dentsc@usc.edu or 213-740-9356.

Log In Options

- USC NetID: Active users with a @usc.edu address can use their USC NetID login option. If this does not work, you may still use your original D2L credentials described below

USC NetID Login
CLASS WEBPAGE
DEN D2L (Desire 2 Learn)
https://courses.uscden.net/d2l/login
LEC / DIS WEBCASTS
ASSIGNMENTS
ANNOUNCEMENTS
OFFICE HOURS
Ed Discussion
EMAIL
Zoom Videos for the non-DEN lecture and discussion are posted at the EE457 merged course on blackboard.usc.edu under USC Zoom Pro Meeting

**Non-DEN LECTURE:**
(a) 02:00-3:50PM  MW OHE230

**Non-DEN DISCUSSION:**
(b) 2:00- 2:50PM  F   CPA102
Before trying to join an any USC course Zoom meeting (DEN or non-DEN), first login to your blackboard.usc.edu to authenticate that you belong to USC.

Then you can login to usc.zoom.us using your single-sign-on (SSO)

Click on sign-in
How do you join EE457 Zoom meeting?

1. For DEN Lecture or DEN Discussion
   Go to the EE457 course page on D2L.

https://courses.uscden.net/d2l/home/22075
How do you join EE457 Zoom meeting?

2. For non-DEN Lecture or non-DEN Discussion

Go to the EE457 course page on Blackboard => USC Zoom Pro Meeting

<table>
<thead>
<tr>
<th>Start Time</th>
<th>Topic</th>
<th>Meeting ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Today (Recurring)</td>
<td>EE457 Lecture 2:00-3:50 PM MW Puvvada</td>
<td>977 4510 9260</td>
</tr>
<tr>
<td>2:00 PM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wed, Jan 12 (Recurring)</td>
<td>EE457 Lecture 2:00-3:50 PM MW Puvvada</td>
<td>977 4510 9260</td>
</tr>
<tr>
<td>2:00 PM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fri, Jan 14 (Recurring)</td>
<td>EE457 Discussion 2:00PM Fri Zhijun/Srikant h/Ayush</td>
<td>945 9480 3017</td>
</tr>
</tbody>
</table>
Verilog language and ModelSim Simulator

INTRO. LECTUREs are posted
Buy the textbook from the Bookstores or any online source

TEXTBOOK
Computer Organization & Design - The Hardware and Software Interface 5th edition (or 4th edition (Revised Printing))
By D. A. Patterson (Berkeley) and J. L. Hennesy (Stanford)

CLASS NOTE
pdf files are available online. Download and annotate

Lab Manual
.pdf files will be posted progressively on the BB
Understand,
No need to memorize,
Learn to design.

Demonstrate your understanding in the exam

Plenty of hours of office hours per week
Grades
Grades

- Very easy to get an A grade
Grades

• Very easy to get an A grade

• Equally easy to get a F grade
# Grades of Fall 2021

www-classes.usc.edu/engr/ee-s/457/ee457_Fall2021_exams/ee457scores_total_Fall2021.htm

<table>
<thead>
<tr>
<th>Grade</th>
<th># of Students</th>
<th>%</th>
<th>% Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Extraordinary</td>
<td>39</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Superior</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>63</td>
<td>42.3%</td>
<td>57.0%</td>
</tr>
<tr>
<td>A-</td>
<td>22</td>
<td>14.8%</td>
<td></td>
</tr>
<tr>
<td>B+</td>
<td>21</td>
<td>14.1%</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>14</td>
<td>9.4%</td>
<td></td>
</tr>
<tr>
<td>B-</td>
<td>13</td>
<td>8.7%</td>
<td></td>
</tr>
<tr>
<td>C+</td>
<td>4</td>
<td>2.7%</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>3</td>
<td>2.0%</td>
<td></td>
</tr>
<tr>
<td>C-</td>
<td>4</td>
<td>2.7%</td>
<td></td>
</tr>
<tr>
<td>D+</td>
<td>2</td>
<td>1.3%</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>1</td>
<td>0.7%</td>
<td></td>
</tr>
<tr>
<td>D-</td>
<td>1</td>
<td>0.7%</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>1</td>
<td>0.7%</td>
<td></td>
</tr>
<tr>
<td><strong>SubTotal</strong></td>
<td><strong>149</strong></td>
<td><strong>100.0%</strong></td>
<td><strong>100.0%</strong></td>
</tr>
<tr>
<td><strong>DROP</strong></td>
<td><strong>1</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>150</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Extract from your syllabus

Two scales will be used to divide scores between Final exam and the earlier exams

<table>
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<tr>
<th>Exams</th>
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We appreciate your efforts

- ~50% of the class gets an A grade

No place for the lazy and uninterested

- ~10% of the class fails or drops
There is no competition. Everyone can get an A grade.

You need to aspire for it, and work for it.

You get what you worked for.

No grace grade (No minimum grade).
Undergraduates
Please do not take it easy

- First five weeks, in the RTL design area, you have an advantage.

- But in the remaining 10 weeks, if you slacken, you end up with a C or a D 😞
Academic Integrity

- Very Important
- Do not take it easy
- You can work with your lab partner on labs, but both need to participate
- Homeworks and lab reports are individual effort items
- Do not copy lab codes. You can easily get caught!
- We are here to help, so there is no need to cheat.
Download the lab exercises and work on them. Do not get them from your seniors.
New students (new to USC)

• You have a lot to catch up
• Make up for any deficiency in the logic design area (EE354L area)
• First three weeks are crucial to survive! 
  EE457 Study Plan for first 3 weeks.pdf

• Get to know
  – Verilog HDL
  – Modelsim/Questasim simulator
  – Login to viterbi-scf1.usc.edu or viterbi-scf2.usc.edu
  – Use Xwin-32 (on Windows) or Xquartz (on Max OS X)
  – Get to know to access and use VDI
  (mydesktop.usc.edu)
ssh PuTTY on windows to login to viterbi-scf1.usc.edu
OpenSSH on Mac to login to
viterbi-scf1.usc.edu or viterbi-scf2.usc.edu

Using OpenSSH to Connect to Mizar via SSH (Macintosh)

1. Open the Utilities folder within the Application folder.
2. Double-click the Terminal icon.
3. A window will display the following information:
Learn to run QuestaSim on viterbi-scf1/viterbi-scf2 Linux servers

(a) using X-Win32 on your Windows laptop
or
(b) using XQuartz on your Mac running Mac OS X
VDI (myDesktop.usc.edu)
VDI (myDesktop.usc.edu)
Generally do **vpn** to USC when you work from home.

However, there is no need to do vpn, if you are accessing VDI from home.
Get to know to use Questasim on Linux servers or VDI
Get to know to use Questasim on VDI or Modelsim on Linux