Homework Assignment #1 Solution
EE 477 Fall 2007

6. \( \text{Output} = \overline{E} \cdot (ABC + BCD + ACD + ABD) \)

Logic representation:

We only allow using NOR, NAND, NOR, INV. Thus, apply the following steps.
I. We add some inverters which are represented by a couple of circles as shown in the following.

II. Then, we apply De Morgan’s law.
III. Transistor-level circuit.

It requires 38 transistors
2. 1) Redesign your design from Problem 6 at the transistor level using a compound gate.

\[ \text{Output} = \bar{E} \cdot (ABC + BCD + ACD + ABD) = \bar{E} \cdot (BC(A + D) + AD(C + B)) \]

2) Using only NAND gates.

We apply De Morgan’s law to satisfy the requirement. Do the following:

Step 1
Step 2

3-input NAND gate has 6 transistors.
2-input NAND gate has 4 transistors.
4-input NAND gate has 8 transistors.

Transistor count = 4 \times (3\text{-input NAND}) + 3 \times (2\text{-input NAND}) + 1 \times (4\text{-input NAND})
= 4 \times 6 + 3 \times 4 + 1 \times 8 = 44 \text{ (Transistors)}

Step 3

Transistor Count Comparison Table

<table>
<thead>
<tr>
<th>Problem #</th>
<th>Problem #6</th>
<th>Problem #7(a)</th>
<th>Problem #7(b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor #</td>
<td>38</td>
<td>20</td>
<td>44</td>
</tr>
</tbody>
</table>
8. Sketch a stick diagram of a transmission gate 2-input mux.
Let’s first look at the transistor level design.

<table>
<thead>
<tr>
<th>S</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>A</td>
</tr>
<tr>
<td>1</td>
<td>B</td>
</tr>
</tbody>
</table>

The following is its stick diagram.