1. 3-input MUX

Boolean expression for \( \text{mux}_\text{out} \):

\[
\text{mux}_\text{out} = \overline{\text{clk} \cdot S \cdot \text{Do}} + \overline{\text{clk} \cdot S \cdot \text{Di}} + \text{clk} \cdot \text{Q}
\]

= \frac{\overline{\text{clk} \cdot S \cdot \text{Do}} + \overline{\text{clk} \cdot S \cdot \text{Di}} + \text{clk} \cdot \text{Q}}{\text{clk} \cdot S \cdot \text{Do} + \text{clk} \cdot S \cdot \text{Di} + \text{clk} \cdot \text{Q}}

Mux design with NAND, INVERT gates

Mux design with NOR, INVERT gates

Latch design

When set = 1, Q = 1, \( \bar{Q} = 0 \)

When reset = 1, Q = 0, \( \bar{Q} = 1 \) (when \( \text{clk} = 1 \))

Set asynchronously

Reset synchronously
2. Mux design with transmission gates

In Problem 1, we use:

6 INVERT \rightarrow 12 transistors
3 3-NOR \rightarrow 18 transistors
1 2-NOR \rightarrow 4 transistors

\{ \begin{align*}
\text{34 transistors total}
\end{align*} \}

Here, we use:

2 INVERT \rightarrow 4 transistors
4 transmission gate \rightarrow 8 transistors

\{ \begin{align*}
\text{12 transistors total, LESS.}
\end{align*} \}
3. \[ \text{out} = (C+D+E) \cdot (F+GH) \]

For nmos transistor, source is the lower potential node (closest to GND).

For pmos transistor, source is the higher potential node (closest to VDD).

4. \[ \text{fox, via} 2, \text{via} 3, \text{via} 4 \]

- fox: field oxide
- via 2: via between m2 & m3
- via 3: via between m3 & m4
- via 4: via between m4 & m5
Assume thin oxide is already there.

1. deposit polysilicon using CVD (chemical vapor deposition)

2. deposit positive photoresist onto polysilicon

3. expose to UV light through photomask. (initial patterning of photoresist)

Positive PR is initially insoluble, after exposed to UV light it becomes soluble.

4. treated, soluble photoresist is removed by special solution called developer.

5. etch away exposed polysilicon with wet or dry etching

6. remove the remaining photoresist by plasma containing oxygen.
6. To make the PN junction (formed between Pt diffusion and n-well) is reverse biased, so no current will flow from Pt to n+.

7. poly : oxide

poly
Pt
n+
metal 1

m1

ox: nwc/ox: pdc

ox: ndc: ox: psc: ox

nwc - n well contact
pdc - p diffusion contact
ndc - n diffusion contact
pc - poly contact

8. These bipolar parasitic transistors are formed among Pt diffusion - nwell - P-substrate (PNP) and n+ diffusion - P-substrate - nwell (NPN).

9. If the metal wire width is too narrow, it is possible the wire will break during fabrication process or afterwards. To avoid this open circuit problem, we have the minimum width for metal.