β_n = 4.3 β_p and the NMOS transistors are unit size transistor so we have W_n = 4λ and L_n = 2λ and we take L_p = L_n = 2λ

\[
β_{neff} = \beta_n \frac{W_n}{L_n} \quad \beta_{peff} = \frac{1}{7} \beta_p \frac{W_p}{L_p} = \frac{1}{7 \times 4.3} \beta_n \frac{W_p}{L_p}
\]

At the worst case rise and fall time we want:

rise time = 2*fall time \rightarrow R_{eff} (pull up) = 2*R_{eff} (pull down) \rightarrow 2*β_{peff} = β_{neff}

\[
2 \times \frac{1}{7 \times 4.3} \beta_n \frac{W_p}{L_p} = \beta_n \frac{W_n}{L_n} \Rightarrow W_p = 15.05 \quad W_n = 15.05 \times 4\lambda = 60.2\lambda \quad (60\lambda \text{ is used})
\]

1-b)
2) 

\[ \beta_n = 4.3 \beta_p \text{ and for the smallest transistor (PMOS) we have } W_p = 8 \lambda \text{ and } L_p = 2 \lambda \text{ and we take } L_p = L_n = 2 \lambda \]

\[ \beta_{neff} = \frac{1}{5} \beta_n \frac{W_n}{L_n} \quad \beta_{peff} = \beta_p \frac{W_p}{L_p} = \frac{1}{4.3} \beta_n \frac{W_p}{L_p} \]

\[ \beta_{peff} = \beta_{neff} \Rightarrow \frac{1}{5} \beta_n \frac{W_n}{L_n} = \frac{1}{4.3} \beta_n \frac{W_p}{L_p} \Rightarrow W_n = 1.16 \quad W_p = 1.16 \quad (8\lambda) = 9.3\lambda \quad (9\lambda \text{ is used}) \]

Worst case fall happens we go from ABCDE=1110 to 11111 and worst case rise happens when we go from ABCDE=11111 to 11110

![Diagram of a circuit](image)

3) 

NMH = 2.2 - 2 = 0.2 V

NML = 0.3 - 0.2 = 0.1 V

The circuit would work correctly even with a noise signal which has a plus or minus 0.04 V swing.
4)

4-a)

<table>
<thead>
<tr>
<th></th>
<th>Aᵢ</th>
<th>Bᵢ</th>
<th>Cᵢ₋₁</th>
<th>Ci_bar=Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>Worst Case Rise</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Previous</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Present</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

4-b)

We have an inverter with: \( W_n = 4\lambda \) \( \quad \) \( L_n = 2\lambda \) \( \quad \) \( W_p = 16\lambda \) \( \quad \) \( L_p = 2\lambda \)

\[
\beta_{n_{\text{eff}}} = \frac{1}{2} \beta_n \frac{W_n}{L_n}
\]

and we want \( \beta_{n_{\text{eff}}} = \beta_n^4 \) \( \Rightarrow W_n = 2 \times 4\lambda = 8\lambda \)

\[
\beta_{p_{\text{eff}}} = \frac{1}{2.5} \beta_p \frac{W_p}{L_p}
\]

and we want \( \beta_{p_{\text{eff}}} = \beta_p^{4+4} \) \( \Rightarrow W_p = 2.5 \times 16\lambda = 40\lambda \)

4-c)

PMOS transistor with A (Aᵢ in schematic) input can be, in the worst case, in the path with two PMOS transistors in series which can happen when ABC=001 or ABC=010

The Path with A will have B or C in it which have already been sized to 40\(\lambda\) (which assume can be represented with R for effective channel resistance)

The overall pull up worst case path has 2.5 PMOS transistors in series (ABC=100)

\[
2.5R = R(B) + R(A) = R + R(A) \Rightarrow R(A) = 1.5R \Rightarrow W_p(A) = \frac{40\lambda}{1.5} = 26.6\lambda \text{ (We can use } 26\ \lambda)\]
Diffusion Capacitances Charged = 13

Diffusion Capacitances Discharged = 15
4-e)
\[ R_{\text{total}} = R_{\text{chn}}(B) + R_{\text{chn}}(C) + 0.5R_{\text{chn}}(B) \]
\[ R_{\text{chn}}(C) = R_{\text{chn}}(B) = 0.5 \times R_{\text{chn}}(\text{Unit size}) \]
\[ R_{\text{total}} = 2.25 \times R_{\text{chn}}(\text{Unit size}) \]

\[ C_{\text{total}} = 8C_{dp} + 5C_{dn} \]

\[ RC(\text{Lumped}) = R_{\text{total}} \times C_{\text{total}} = \left[ 0.5 \times R_{\text{chn}}(\text{Unit size}) \right] \times \left[ 8C_{dp} + 5C_{dn} \right] \]

5)
NMOS: \( W_n = 3 \times 3\lambda \) and \( L_n = 2 \times 2\lambda \)

\[ C_g = \varepsilon_0 \varepsilon_{\text{ox}} \frac{A}{d} \]
\[ C_g = 8.85 \times 10^{-14} \text{F/cm} \times 3.9 \times 3 \times 3 \lambda \times 2 \times 2 \lambda = 8.53 \times 10^{-14} \text{F} \]
\[ = 3.1390 \times 10^{-15} \text{F} = 3.139 \text{fF} \]

6)
\( W = 10\lambda \) \( L = 4\lambda \)
\[ P = (2(4\lambda) + 10\lambda) \times 0.120 \mu = 2.16 \mu \]
\[ A = (0.1\mu) \times (10\lambda \times 0.120 \mu) + 4\lambda \times (10\lambda \times (0.120 \mu)^2) = 4.92 \mu \]
\[ C_d = C_{jbsn} \times A + C_{jbswn} \times P = 17.27 \times 4 \mu F/\mu^2 \times 4.92 \mu^2 = 84.96 \mu F + 9.007 \mu F = 93.96 \mu F \]

7)
\( V_{dd} = 2.5 \text{ V} \)
\[ V_{in} = 1.55 > \frac{V_{dd}}{2} \Rightarrow \left| \frac{\beta_p}{\beta_n} \right| > 1 \]
@ region D we have NMOS in Linear and PMOS in Saturation.

Vin=1.6V      Vdd=2.5V

**NMOS:** (We want the NMOS to stay ON and in Linear region)

1)  On Condition: \( V_{gs} > V_{th} \) \( 1.6 > 0.7 \) (Condition is met regardless of the Vout value)
2)  Linear Condition: \( V_{ds} < V_{gs} - V_{th} \) \( \Rightarrow V_{out} < 1.6 - 0.7 \) \( \Rightarrow V_{out} < 0.9 \) (*)

**PMOS:** (We Want the PMOS to stay ON and in Saturation region)

1)  On Condition: \( V_{gs} < V_{th} \) \( -0.9 < -0.7 \) (Condition is met regardless of the Vout value)
2)  Saturation Condition: \( V_{ds} < V_{gs} - V_{th} \) \( \Rightarrow (V_{out} - V_{dd}) < (1.6 - V_{dd}) - (-0.7) \) \( \Rightarrow V_{out} < 2.3 \) (**)

(*) and (**) \( \Rightarrow \) in order to remain in D region \( V_{out} < 0.9 \)