EE477 HW#6 Solution  
Fall 2008

Due Date 11/23/2008

Problem 1

\[ \tau = R_{chn}(C_{d(n+p)} + C_{dint} + C_{mint} + C_{pad}) + \\
R_{dint}(C_{dint} + C_{mint} + C_{pad}) + (R_{contact} + R_{mint})(C_{mint} + C_{pad}) \]

\[ R_{mint}(4\lambda) = 570\Omega \]
\[ R_{mint}(8\lambda) = 285\Omega \]

Also, \( C_{mint} \) will be twice as large in the \( 8\lambda \) circuit (area in parallel plate model will be twice as large).

\[ \tau(4\lambda) = 1.22 \times 10^{-9}s = 1.22ns \]
\[ \tau(8\lambda) = 1.36 \times 10^{-9}s = 1.36ns \]

The \( 4\lambda \) metal circuit is faster by about \( .14ns \).
Problem 2

In the first case:

\[ \tau_1 = R_{tot} \cdot C_{tot} = 2602 \Omega \cdot 559 \times 10^{-15} F = 1.45 \text{ns} \]

\[ \tau_2 = R_{tot} \cdot C_{tot} = 2317 \Omega \cdot 641 \times 10^{-15} F = 1.48 \text{ns} \]

Problem 3

\[ C_L = C_{d(n+p)} + C_{dint} + C_{mint} + C_{pad} = 559.06 fF \]

\[ t_f = \int_{V_{IDD}}^{V_{DD}-V_{tn}} \frac{-C_L}{I_{DSSAT}} dV_{out} + \int_{V_{IDD}}^{V_{DD}-V_{tn}} \frac{-C_L}{I_{DSLIN}} dV_{out} \]

\[ = t_{f1} + t_{f2} \]

\[ \beta_{Neff} = \beta_N \cdot \frac{3 \cdot 4}{2} = 6 \beta_N \]

\[ t_{f1} = \frac{2C_L(V_{tn} - 1.1V_{DD})}{\beta_{Neff}(V_{DD} - V_{tn})^2} = 2.36 \times 10^{-10} s \]

\[ t_{f2} = \frac{C_L}{\beta_{Neff}(V_{DD} - V_{tn})} \left( \ln \left[ \frac{19V_{DD} - 20V_{tn}}{V_{DD}} \right] \right) = 0.6123 \times 10^{-9} s \]

\[ t = 8.4830 \times 10^{-10} \times 10^{-10} s = 0.848 \text{ns} \]

Problem 4

This is now a wire in isolation. We used the lumped wire delay model.

a) \[ \tau = 0.69RC = 0.69 \cdot R_{mint} \cdot C_{mint} = 3.23 \times 10^{-11} s = 32.3 \text{ps} \]

b) \[ \tau = 0.69RC = 0.69 \cdot R_{mint}/2 \cdot C_{mint} \cdot 2 = 3.23 \times 10^{-11} s = 32.3 \text{ps} \]

These are both delays (50% → 50%) so a fall time would be about twice the delay.
Problem 5

We will now use the distributed wire delay model.

\[
t = \frac{.7rc^2}{2} = \frac{.7}{2} \cdot 0.1178 \frac{\Omega}{\mu} \cdot 0.0172 \times 10^{-15} \frac{F}{\mu} \cdot (4755\mu)^2
\]

\[
= 1.60 \times 10^{-11} = 16\text{ps}
\]

This time is about 16ps less than the lumped time.

Problem 6

The capacitance including fringing fields is between 2.5 and 3 times the $C_{pp}$ parallel plate capacitance of $82fF$.

\[
2.5 \cdot 82fF = 205fF, \quad 3 \cdot 82fF = 246fF.
\]

Problem 7

Equivalent circuit for Prob 7. The red circle is the output of the NAND3 gate, the blue circle is the input to an inverter.
Using the distributed model, we calculate the delay at the output of the NAND3 as:

\[
\tau = R_{chn}(23C_d + 6C_g) + R_{chn}(21C_d + 6C_g) + R_{chn}(19C_d + 6C_g) + R_{chn}(17C_d + 6C_g) \\
= 2.88 \times 10^{-9} s = 2.88 \text{ns}
\]

The delay at the input of an inverter is:

\[
\tau = R_{chn}(23C_d + 6C_g) + R_{chn}(21C_d + 6C_g) + R_{chn}(19C_d + 6C_g) + R_{chn}(17C_d + 6C_g) + \frac{R_{chip} R_{chn}}{R_{chip} + R_{chn}} (2C_d + 2C_g) \\
= 2.98 \times 10^{-9} s = 2.98 \text{ns}
\]

**Problem 8**

Since \( C_d = C_g \), we use \( a = 4 \).

\[
n = \frac{\ln \left( \frac{C_d}{C_g} \right)}{\ln 4}
\]

\[
\frac{\ln \left( \frac{4 \times 10^3 \mu F}{5 \mu F} \right)}{\ln 4} = 4.8 \approx 5
\]

**Problem 9**

Ernie’s Boss’ Design
\[ R_{wire} = 0.025 \Omega \left( \frac{9 \times 10^{-3}}{3 \times 0.125 \times 10^{-6}} \right) = 600 \Omega \]

\[ C_{wire} = \left( \frac{50 \times 10^{-15}}{1 \times 10^{-3}} \right) 9 \times 10^{-3} = 4.5 \times 10^{-13} F \]

Ernie’s Boss’ design has three stages.
Stage 1 (Stage 3 is equivalent):

\[ RC_1 = R_{CHP}(2C_d + C_{wire}/3 + 2C_g) + R_{wire}/3(C_{wire}/3 + 2C_g) \]
\[ = 5.0 \times 10^{-10} s \]

\[ RC_2 = R_{CHN}(2C_d + C_{wire}/3 + 2C_g) + R_{wire}/3(C_{wire}/3 + 2C_g) \]
\[ = 1.775 \times 10^{-10} s \]

\[ RC_{tot} = 2 \cdot RC_1 + RC_2 = 1.1775 \times 10^{-9} s \]

Ernie’s Design:

\[ RC = R_{CHP}(2C_d + C_{wire} + 2C_g) + R_{wire}(C_{wire} + 2C_g) \]
\[ = 1.12 \times 10^{-9} \]

\[ \therefore \text{Ernie’s Boss’ design is faster by 0.05us.} \]