Hw 2 Solution

1.

We need to design a counter that counts upto 5 and resets to zero if count is enabled.
We keep count as a part of the flip flop and allow the value to be passed when count is enabled else
the second latch of the FF will circulate the old value.

The truth table for the counter will be as follows:

D0 D1 and D2 are the next states for the counter and Q0 Q1 Q2 are the present state inputs

<table>
<thead>
<tr>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>x</td>
<td>x</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Solving using KMap for D3 D2 and D1 with Q3 Q2 and Q1 as variables we get
\[
D_2 = \overline{g_1} \overline{g_0} + g_2 \overline{g_0}
\]

\[
D_7 = \overline{g_2} \overline{g_1} g_0 + g_1 \overline{g_0}
\]

\[
D_0 = \overline{g_0}
\]
The schematic for the counter is
The schematic for the individual FF is
For the FF shown above the first latch uses a mux using Transmission gates which used 8 transistors.

Implementing the same Mux using NAND NOR INVERT

Here D is the input to the latch and Q is the output of the latch which needs to be circulated.

Total Transistors = 6 + 4 + 4 + 6 = 20
3. 

\[ \text{notcredit} = \left\{ \left( \text{attendingclass} + \text{watchingonDEN} \right) \ast \left( \text{readingthetext} \ast \left( \text{doinghomework} \ast \text{workingoldhomeworkproblems} \right) \right) \right\} + \text{tooksimilarclass} \]
4. Cross section is as follows

\[ C = \text{Contact cut} \]
5. Layers such as Active layers (n and p), Polysilicon, Metal layers (1 and higher) and silicon dioxide (sio2), contacts and vias

6. A p+ is found in a p- substrate when we want to tie the substrate to gnd using a Ptap

7.

8. There is the possibility of permanent damage to the metal connections due to the high current flow

9. To avoid mask misalignment problems we have design rules which provide minimum spacing requirements and minimum width requirements