Given $V_{tp} = -1\text{V}$, $V_{tn} = 1\text{V}$, $\frac{\beta_n}{\beta_p} = 0.9$.

Find $V_{in}$.

Since both PMOS and NMOS are in SAT, so the inverter is in region $C$. In region $C$, there is only one value of $V_{in}$.

Current of PMOS in SAT is:

$$I_{dsP} = \frac{\beta_p}{2} \left[ V_{in} - V_{tp} - V_{tp} \right]$$

$$V_{tp} = 5\text{V}$$

Current of NMOS in SAT is:

$$I_{dsN} = \frac{\beta_n}{2} \left[ V_{in} - V_{tn} - V_{tn} \right]$$

$$V_{tn} = 0\text{V}$$

with $I_{dsP} = -I_{dsN}$

$$V_{in} = \frac{V_{tp} + V_{tp} + V_{tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

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$$V_{in} = 5 + (-1) + 1 \times \sqrt{0.9}$$

$$1 + 0.9$$

$$= 2.54\text{V}$$
2. Given $V_{gs} = -2.9\,V$, $V_{tp} = -1\,V$
Find range of $V_{gs}$

Since transistor is in linear region, so $V_{gs} > V_{gs} - V_{tp}$

$V_{gs} > -2.9 - (-1)$
$V_{gs} > -1.9\,V$

Therefore, $V_{gs}$ must be greater than $-1.9\,V$ to be in linear region.

3. Given $V_{gs} = 2.1\,V$, $V_{ds} = 1.4\,V$, $V_{en} = 1\,V$

$V_{gs} > V_{en}$ \(\text{and} \) \(2.1\,V > 1\,V\) \(\text{Yes}\)
$V_{ds} > V_{gs} - V_{en}$ \(\text{and} \) \(1.4\,V > 2.1\,V - 1\,V\) \(\text{Yes}\)

Therefore, the transistor is in SAT

Now $V_{gs} = 4.1\,V$ and $V_{gs} = 2.6\,V$

$V_{gs} > V_{en}$ and $V_{gs} < V_{gs} - V_{en}$

So the transistor is in linear region.
A. \[ I_{on} \propto (V_{gs} - V_{th}) \]

If \( V_{gs} \) increases, \( I_{on} \) decreases for some values of \( V_{gs} \) and \( V_{th} \).

The threshold voltage \( V_{th} \) increases due to body effect, and body effect occurs when its source voltage is not zero or not connected to ground.

The transistors with a tick (\( \checkmark \)) are subject to the body effect.
At $t = 0$, $V$ rises from 0 to 3V instantaneously.

At $t = 0^+$, $V_{GS} = 3V - 4V = -1V$  
$V_{DS} = 5V - 4V = 1V$

The NMOS is subjected to body effect because its source voltage is not zero.

Assume $V_{TH, body-effect} = 1.5V$

Since $V_{GS} = -1V < V_{TH, body}$, so the NMOS is in cut-off region at $t = 0^+$.

After some time $V_{out} = 5V$ (remember a PMOS transfer good one).

At $t = \infty$, $V_{GS} = 3V - 5V = -2V$  
$V_{DS} = 5V - 5V = 0V$

$V_{GS} = -2V < V_{TH, body}$, so the NMOS is still in cut-off region at $t = \infty$. 
7. \( V_{in} = 0 \text{V} \)
\( V_{out} = 2 \text{V} \)

\[ V_{GSP} = 0 - 2 = -2 \text{V} \]
\[ V_{ISP} = 0 - 2 = -2 \text{V} \]
(assume \( V_{P,1000} = -1.5 \text{V} \))

\[ V_{GSP} = -2 < V_{P,1000} = -1.5 \text{V} \]
\[ V_{ISP} = -2 < V_{ ISP - V_{P,1000}} = -2 - (-1.5) = -0.5 \text{V} \]

Hence, the PMOS is in SAT

\( V_{out} \) will keep dropping until the transistor enters cut-off region when \( V_{GSP} = V_{P,1000} \)

\[ V_{ISP} = V_{GSP} - V_{out} = V_{P,1000} \]
\[ V_{out} = V_{GSP} - V_{P,1000} \]
\[ = 0 - (-1.5) \]
\[ = 1.5 \text{V} \]

\[ \therefore \text{ the final } V_{out} = 1.5 \text{V} \]
8. \( V_{in} = 0V \)

\[ V_{D} = 2V \]

\[ V_{ss} = 5V \]

\[ V_{in} = 5V - 0V = 5V \]
\[ V_{ss} = 2V - 0V = 2V \]
\[ \text{Assume } V_{en} = 1V \]

\[ V_{in} > V_{en} \]
\[ V_{en} < V_{in} - V_{en} = 5V - 1V = 4V \]

\[ \Rightarrow \text{ The NMOS is in linear region} \]

\[ V_{out} \text{ will keep dropping until } 0V \text{ because the transistor is always "ON" (} V_{en} \text{ is always larger than } V_{in} \text{). Note that an NMOS transistor good zero.} \]

\[ \Rightarrow \text{ The final } V_{out} = 0V. \]
9. The Noise Margin = \( V_{oh\text{-max}} - V_{ol\text{-min}} \)
\[ = 3.5V - 3.4V = 0.1V \]

... if the noise amplitude is \(< 0.05V\), there will be no noise problem.
If the noise amplitude is \(< 0.8V\), there will be a noise problem.