1. Cadence schematic

2.
   a) 

\[ V_{g} = 2.5 \text{V} \]
\[ V_{i}n = 2.5 \text{V} \]
\[ V_{o}u = 0 \text{V} \]

Assume \( V_{g} \) is 2.5V and \( V_{i}n \) is 2.5V. \( V_{o}u \) is 0V at \( t=0^+ \).
Initially the NMOS pass transistor is not subject to body effect since \( V_{s} = 0 \text{V} \). However, once \( V_{s} \) is no longer at 0V there is body effect on the NMOS.

\[ @ t = 0 \]
\[ V_{g}sn = 2.5 \text{V} > V_{tn} = 0.6 \text{V} \rightarrow \text{NMOS is on.} \]
\[ V_{dsn} (= 2.5 \text{V}) > V_{g}sn - V_{tn} (=1.9 \text{V}) \rightarrow \text{NMOS is in saturation.} \]

\[ @ t = \text{infinity} \]
\[ V_{g} = 2.5 \text{V} \]
\[ V_{i}n = 2.5 \text{V} \]
\[ V_{o}u = 1.7 \text{V} \]

\( V_{s} \) is rising until \( V_{g}sn \) reaches \( V_{tn,be} (= 0.8 \text{V}) \)

\[ @ t = \text{infinity} \]
\[ V_{g}sn = V_{tn,be} = 0.8 \text{V} \rightarrow \text{NMOS is cutoff} \]
\[ V_{o}u = V_{s} = 2.5 - 0.8 = 1.7 \text{V} < V_{i}n (=2.5 \text{V}) \]

Therefor, NMOS transfers a weak 1 because it’s cutoff when \( V_{g} < V_{tn} \).

b) We can observe from part a) body effect makes the 1 weaker (makes it worse to transfer a 1.)

3.

\[ A(0,11) \]
\[ B(0,7) \]
\[ C(1,8) \]
\[ D(8,12) \]
\[ E(6,7) \]
\[ F(6,7) \]
\[ E(9,11) \]
4. The advantage of using material with a higher dielectric constant is that we can avoid gate leakage problem happened in thin gates. Gates use thicker dielectrics leak less.

5. 
\[ V_{dsn} = 0.2 \text{V}, \quad V_{gsn} = 1.7 \text{V}, \quad V_s = 0 \text{V} \text{ (no body effect,) } V_{tn} = 0.6 \text{V} \]
\[ \beta_n = 219.4*(W/L) \]
\[ V_{gsn} > V_{tn} \to \text{NMOS is on.} \]
\[ V_{dsn} (=0.2\text{V}) < V_{gsn} - V_{tn} (=1.7\text{V} - 0.6\text{V}) \to \text{NMOS is in linear region of operation.} \]
\[ I_{dsn} = (\beta_n/2)[2(V_{gsn} - V_{tn}) V_{dsn} - V_{dsn}^2] = (219.4/2)*(24/3)*(2*1.1*0.2 - 0.2^2) = 351.04 \mu\text{A/V}^2 \]

6. 
\[ V_{dsp} = -0.8 \text{V}, \quad V_{gsp} = -1.6 \text{V}, \quad V_s = 2.5 \text{V} \text{ (no body effect,) } V_{tp} = -0.6 \text{V} \]
\[ |V_{gsp}| > |V_{tp}| \text{ (or } V_{gsp} < V_{tp}) \to \text{PMOS is on.} \]
\[ |V_{dsp}| < |V_{gsp}| - |V_{tp}| \text{ (or } V_{dsp} > V_{gsp} - V_{tp}) \to \text{PMOS is in linear region of operation.} \]
\[ R_{eff} = \frac{1}{\beta_p(|V_{gsp}| - |V_{tp}|)} = \frac{1}{51\frac{W}{L} (\mu\text{A/V}^2) \cdot 1(V)} = 10^6 \cdot \frac{L}{W} \text{ (} \Omega \text{)} \]

7. “C” point occurred at \( V_{in} = 0.95 \text{V} < V_{dd}/2 (=1.25 \text{V}) \) implies that the transfer curve shifts to the left which means \( |\beta_n| > 1 \text{ or } |\beta_p| < 1. \)

8. 
Given \( V_{in} \), we know \( V_{gsn} \) & \( V_{gsp} \).
Given the sizes of the transistors, we know \( \beta_n \) & \( \beta_p \)
Given inverter is on segment B (NMOS is in saturation region and PMOS is in linear region,) we can set up the current equations for both transistors.
\[ I_{dsp(lin)} = -(\beta_p/2)[2(V_{gsp} - V_{tp}) V_{dsp} - V_{dsp}^2] \]
\[ I_{dsn(sat)} = (\beta_n/2)[(V_{gsn} - V_{tn})^2] \]
\[ I_{dsp(lin)} = -I_{dsn(sat)} \to \text{Solve for } V_{dsp} \to V_{out} = V_{dd} + V_{dsp} \]