1. Flip Flop that can be Reset (you could make one that could both be set and reset)

Flip Flop that can be Set
Beck Counter

C4
C3
C2
C1

FF4
Q
reset
D
clock

FF3
Q
reset
clock

FF2
Q
reset
D
clock

FF1
Q
set
clock

reset

set

clock

clock

clock
The logic equation for the multiplexer used for the latch is

(\overline{\text{/}} \text{ stands for invert})

Out = D(\text{clock} \cdot \text{count}) + [(Q)(\overline{\text{clock}} + \text{count})]

Using Boolean laws we can convert the above equation to

Out = \overline{(A \cdot B)}

Where A= \overline{(D \cdot \text{clock} \cdot \text{count})} \quad B=\overline{(Q \cdot (\overline{\text{clock} \cdot \text{count}}))}

We can see that expression A is a 3 input NAND gate and expression B is a series of two 2 i/p nand gates. The final expression out is also a 2 i/p NAND gate.

As shown in the figure below

![Diagram](image)

The 2 i/P nand gates take 4 transistors each and the 3 i/p nand gate takes 6 transistors making the total = 18 transistors compared to 8 in the transmission gate based mux
In a negative photolithographic process the unexposed photoresist is removed first.

In a Pwell process the Pwell is tied to Gnd.
7. It can be formed between the n+ diffusion in the pwell, the pwell, (nnp transistor) and the n substrate, or between the p+ diffusion in the n substrate, the n substrate and the pwell (pnp).

8. We are avoiding the possible effect due to the misalignment of a mask leading to the wrong placement of the contact material on the cut, and no contact being made as a result.