Problem 1

a) The pmos is on when $V_{gsp} < V_{tpbe}$ (there is body effect since the source is not connected to Vdd). Then:

$$-0.7 - V_{out} < -0.9$$

$$V_{out} > 0.2V$$

So the pmos will be on until $V_{out} = 0.2V$, then it will not fall any further. If the gate voltage had been 0V, then $V_{out} = 0.9V$, so lowering the gate voltage passed a better zero.

b) An nmos transistor can pass a zero without body effect, but a pmos cannot.

Problem 2

a) 

Vin=1.5V  \hspace{1cm} Vout=1.75V

Figure 1. $t = 0^+$
b) The pmos is on when $V_{gsp} < V_{tpbe}$:

$$0.3V - V_{out} < -0.9V$$

$$V_{out} > 1.2V$$

Since we are only transmitting 1.5V, the pmos will remain ON the entire time. The nmos is on when $V_{gsn} > V_{tnbe}$:

$$2.3V - 1.5 = 0.8 > 0.9$$

This is not true, so the nmos will be CUTOFF.

The region of the pmos will be linear if:

$$V_{dsp} > V_{gsp} - V_{tpbe} - 2.2V > -1.7 + 0.9 = -0.8V$$

True, so the pmos will be LINEAR.

**Problem 3**

A higher dielectric allows the gate oxide to be made thicker and still retain the same capacitance. A thicker gate oxide allows less gate leakage.

**Problem 4**

First, we must find the region of the transistor. The pmos will be linear if:

$$V_{dsp} > V_{gsp} - V_{tpbe}$$

$$-2.2V > -1.7 + 0.9V$$

$$-2.2 > -0.8$$

False, so The transistor is SATURATED, so we use the current equation for saturation:

$$I_{DS} = \beta_P \cdot \frac{W}{L} \left[ \frac{(V_{gs} - V_{tpbe})^2}{2} \right]$$

$$= 51 \times 10^{-6} \text{A/V}^2 \cdot \frac{12}{3} \left[ \frac{(-1.7 + 0.9)^2}{2} \right]$$

$$I_{DS} = 65.28\mu\text{A}$$
Problem 5

Note that there is no body effect here, since the source is connected to constant 0 V.

\[ R = \frac{1}{\beta_{\text{neff}}(V_{gsn} - V_{tn0})} \]

where \( \beta_{\text{neff}} \) = the effective \( \beta_n \).

\[ R = \frac{1}{219.4 \times 10^{-6} A/V^2(2.4 - 0.7)} = 1.78 \times 10^3 \Omega \]

This is assuming that the transistor is minimum size.

Problem 6

nmos linear if:

\[ V_{dsn} < V_{gsn} - V_{tnbe} \]
\[ 0.3 < 1.1 - 0.9 = 0.2 \]

False, the nmos is NOT in linear region.

Problem 7

Firstly, check that the pmos is on. Then, the pmos is linear if:

\[ V_{dsp} > V_{gsp} - V_{tp0} \]
\[ -2.5V > -2.0V + 0.7 = -1.3V \]

This is false, so the pmos is in SATURATION. Also, note that there is no body effect.

Problem 8

The spike occurs at region C, when both transistors are in saturation. If the \( \beta \)'s are equal, this occurs at \( V_{DD}/2 \). Here, region C is occurring to the left of this, so this tells us that the nmos transistor is stronger (it pulls the output down more quickly) so \( |\beta_{\text{neff}}| > |\beta_{\text{peff}}| \).
Problem 9

In region B, the pmos is in the linear region, and the nmos is in the saturation region. Therefore:

\[ V_{dsp} > V_{gsp} - V_{tp0} \]
\[ V_{out} - V_{DD} > V_{in} - V_{DD} - v_{tp0} \]
\[ V_{out} > 1.0 + 0.7 = 1.7V \]

And:

\[ V_{dsn} > V_{gsn} - V_{tn0} \]
\[ V_{out} > V_{in} - v_{tn0} \]
\[ V_{out} > 1.0 - 0.7 = 0.3V \]

The minimum voltage to satisfy both of these conditions is \( V_{out} = 1.7V \).