Energy-Recovery CMOS Design

Jay Moon, Bill Athas*
Univ of Southern California
*Apple Computer, Inc.
jsmoon@usc.edu / athas@apple.com
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Outline

• Motivation
• Review of CMOS switching energetics
• Adiabatic charging
• Energy-Recovery CMOS
• Stepwise charging
• Clock-powered logic (CPL)
• Harmonic resonant charging
• Future Research
Motivation

• It’s becoming increasingly difficult to get rid of the heat generated by VLSI chips
• Battery life for portables
Types of power dissipation

• Dynamic power dissipation
  - Charging and discharging capacitances
  - Short-circuit current

• Static power dissipation
  - Sub-threshold currents
  - Drain-junction leakage
Capacitor energy equations

- Suppose at time $t$, a charge $q$ is transferred from one plate to the other.
- The potential $v$ is $q/C$.
- For a charge transfer increment of $dq$, the additional work is:

$$dE = v dq = \frac{q}{C} dq$$

- For the total charge transfer $Q$:

$$E = dE = \int_0^Q \frac{q}{C} dq = \frac{1}{2} \frac{Q^2}{C}$$

$$Q = CV$$

$$E = \frac{1}{2} CV^2$$
Interestingly (and thankfully) CMOS energetics can be analyzed and understood from the CMOS inverter.

- Charge is conserved
- Energy is conserved
- Neglect leakage current
- Neglect short-circuit current

\[ E_{PS} = VQ = CV^2 \]
The charging event

- Power supply delivers a charge packet of size $Q = CV$
  \[ E_{PS} = CV \cdot V = CV^2 \]
  \[ E_C = (1/2)CV^2 \]
  \[ E_{PS} - E_C = (1/2)CV^2 = E_{HEAT} \]
- This much energy is dissipated in the pFET
The discharging event

- Power supply gets the charge at potential 0
  \[ E_{PS} = 0 \]
- The energy on the capacitor goes from \( (1/2)CV^2 \) to 0
  \[ E_C - 0 = (1/2)CV^2 = E_{HEAT} \]
- This much energy is dissipated in the nFET
- All of the charge is returned to the PS at potential 0
Complex gates and pass logic

- Circuit topology does not change energetics
- It’s about the potential of the charge
- Not where the charge goes
Power supply perspectives

• Inject charge at the highest allowed voltage
  \[ V_{DD} \]
• Recover returned charge at the lowest allowed voltage
  \[ 0 \]
• Simple scheme of shorting capacitors to \( V_{DD} \) or ground through switches
• Maximally wasteful from an energy conservation standpoint
Power equation

- \((1/2)CV^2\) is dissipated to charge the capacitor
- \((1/2)CV^2\) is dissipated to discharge the capacitor
- \(CV^2\) is dissipated per charge/discharge cycle
- If we cycle the capacitor \(F\) times per second:
  \[
P = F \cdot CV^2
  \]

- Power is the rate at which work is done
- Note that if you need to cycle a capacitor \(N\) times from a battery, doesn’t matter if you do it fast or slow.
  The battery is just as dead either way
Voltage scaling

- Energy decreases quadratically with the voltage
  \[ E \sim V_{DD}^2 \]
- Delay increases as the voltage reduces
  \[ \tau \sim \frac{V_{DD}}{(V_{DD} - V_{TH})^2} \]

\[ \frac{\tau_{3.3V}}{\tau_{2.0V}} = 0.3 \]
\[ \frac{E_{3.3V}}{E_{2.0V}} = 2.7 \]

(assuming \( V_{th} = 1V \))
Voltage scaling effects

- PowerMill™ simulations of a 16-bit uProcessor

![Graph 1: Cycle Time vs. Voltage](image1)
![Graph 2: Energy vs. Voltage](image2)
Energy vs. Cycle time

![Graph showing energy vs. cycle time](image_url)
Adiabatic charging

• Charging from a variable-voltage source (e.g. linear ramp)

• Assuming that $R$ is the on-resistance of the switch, the dissipation for charging or discharging $C$ is:

$$E = \frac{RC}{T} \cdot CV^2$$ when $T >> RC$

• Energy can be traded for delay by increasing the charge transport time

• Model the FETs as simple resistors ($R_{up}$ and $R_{dn}$)
Adiabatic-charging principle

Conventional digital CMOS

\[ E_{cycle} = CV^2 \]

Adiabatic charging

\[ E_{cycle} = 2\xi(RC/T)CV^2 \]
Energy-Recovery CMOS

- Exploit the on-chip capacitances of CMOS VLSI to reduce power dissipation below the conventional limit [$FCV^2$] using adiabatic charging and energy-recovery

- This research includes:
  - Clock-energy recovery techniques
  - Clock-powered logic – balanced power versus speed
  - Stepwise charging [charging recycling] technique for
    - Low-power VLSI pin drivers
    - LCD panels
  - Harmonic resonant charging technique for
    - Clock signal for conventional chip
Stepwise charging

- The load C is switched from 0 to V and vice-versa through N steps
- CT should be roughly 10 times larger than C
- Only one supply voltage is required
- Intermediate step voltages converge after a few cycles
- Dissipation for charging or discharging C is: $E = \frac{1}{2}(CV^2)/N$
- The overhead for controlling the FETs needs to be considered
2-Stepwise Driver
2-Stepwise Driver

- Event 1: $1/2C(V/2)^2$ stored, $1/2C(V/2)^2$ dissipated
- Event 2: $1/2C(V/2)^2$ added, $1/2C(V/2)^2$ dissipated
- Event 3: $1/2C(V/2)^2$ recovered, $1/2C(V/2)^2$ dissipated
- Event 4: $1/2C(V/2)^2$ dissipated
- Total dissipation: $1/2C(V/2)^2 \times 4 = 1/2CV^2$
Clock-powered logic

- Exploits adiabatic charging to reduce dissipation
- Uses clocks as global time-varying voltage sources
- The challenge is to use the clock to drive data nodes
Clock-Powered logic design

- Need an efficient clock driver
- Innovate in the design of clock-steering logic
- Use conventional precharged, pass-transistor, static logic
- Use the clock-steering logic for high-capacitance nodes
Resonant clock driver

- Build-up energy in inductor
- Transfer it to the load as a pulse
- Recover the pulsed energy in the inductor
- Repeat the process
The all-resonant clock driver
a.k.a blip driver

- Self-oscillating driver generates almost non-overlapping clock pulses
- Highly efficient because of all-resonant gate drive
- Trade-off between frequency stability and power efficiency
Clocked buffers

- Clock-pass transistor is critical for speed and power performance
- Bootstrapping yields high conductance per gate capacitance
- Clock voltage swing can be decoupled from the logic voltage swing.
  - “Hot clocks”: clock swings above supply
Clocked buffers
Clock-powered logic

- Eliminate pFETs and complements of clocks [smaller circuits, simpler clock requirements]
  - Precharge transistors are hot-clocked nFETs
  - Pass gates in latches are hot-clocked nFETs
- Move more capacitive loads to the clock-powered paths
  - Pass-transistor logic (e.g. in muxes) powered by clocks (not shown)
The AC-1 processor experiment

- Objectives
  - Design and implement low-power processor based on clock-powered logic and blip driver
  - Evaluate significance of blip driver for low-power operation
  - Compare clock-powered processor to conventional, static CMOS alternative

- Approach
  - Select 16-bit ISA
  - Design five-stage pipelined microarchitecture
  - Use energy-recovery latches to inject and retract energy at large capacitive loads
  - Design logic and latches using “mostly-nMOS” circuit styles
  - Include both conventional and blip drivers (for evaluation purposes)
  - Design a implementation of the same ISA using purely conventional static-CMOS techniques
AC-1 microarchitecture

- RISC ISA (Bunda’93)
- 16-bit data
- 16-bit instructions
- 16 registers
- Conventional 5-stage pipeline
- Integer operations only (no multiply or divide)
AC-1 processor

- Clock-powered logic
- Resonant clock driver
- 16-bit data & instructions
- 16 registers
- 0.5um n-well CMOS
- 5-stage pipeline
- ~13K transistors
AC-1c: a conventional processor

- Same target process
- Cascade library cells
- 30k transistors
- 5.5μm²
- Uses gated clocks to reduce power dissipation

- Important differences
  - Custom vs library cells
  - Optimizations
  - Clock gating in AC-1c (40%)
Processor core summary

- **AC-1**
  - First generation clock-powered processor
  - Mostly nMOS logic style
  - Hot clocks
  - Custom layout

- **AC-1c**
  - First generation conventional processor
  - Static CMOS
  - Cascade Epoch standard-cell library

- **ACPL**
  - Second-generation clock-powered processor
  - Static CMOS
  - Low-swing clocks
  - Custom low-power fixed-cell library
  - Cascade Epoch for place and route

- **DC-1**
  - Second-generation conventional processor
  - Static CMOS
  - Single-phase clocking
  - Custom low-power fixed-cell library
  - Cascade Epoch for place and route
Processor comparison

![Processor comparison graph](image)

- ACPL, 6.5x energy recovery
- DC-1
- AC-1/c
- AC-1, no energy recovery
- ACPL, no energy recovery
- AC-1, 6.5x energy recovery
- ACPL, 6.5x energy recovery
Resonant clock drivers

- The difficulty with clock-powered logic is in the clock driver
- Resonant circuits offer the highest efficiency
- Low-power techniques that minimize the switched capacitance in real time do not work well with resonant clock drivers
  - The clocks will vary in phase, amplitude, and pulse width
- Stabilizing the clock load maximizes the capacitive load
- It’s an open research topic
Harmonic resonant charging

- **Sinusoids**
  - Easy and efficient to generate
  - Low overhead
  - Hard to work with, very “undigital”

- **Staircase**
  - Simple to generate and control
  - High overhead
  - Positive-going only

- **Blips**
  - Advantages of the sinusoids
  - Can be complementary
  - Positive-going only

- **Harmonic resonant driver**
  - We thought this would be hard (practically)
  - Now think it is highly doable
Harmonic resonator design

\[ V_{AC} = V_{AB} + V_{BC} \]

Current-fed Guillemin-type network [1948]

Given \( C_L \) and \( f \), find \( L_0, L_1, \) and \( C_1 \) [Moon, 2000]
Harmonic resonator results

- **2\(^{\text{nd}}\) Harmonic Resonator**
  - 85% Energy efficiency
  - 10% slew rate of total cycle time

- **4\(^{\text{th}}\) Harmonic Resonator**
  - 80% Energy efficiency
  - 6% slew rate of total cycle time
Harmonic resonator result

- As R becomes smaller, slew rate decreases while power increases
Harmonic resonator result

- Frequency of output signal doesn’t change for 30% variation of load capacitance while energy efficiency suffers
Future research

• Clock-powered logic and blip driver has been developed as a practical way of exploiting adiabatic charging for CMOS microprocessor

• How about Digital signal processor?
  – Where power goes in DSP?
    • Bus transaction vs. computation

• Energy-recovery SRAM, DRAM, SAM
  – Capacitance variance is minimal because bitlines are dual

• Driving clock network using harmonic resonator
References

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