EE577B Homework #1

8-bit Ripple-Carry Adder Schematic

Due: 9/13/2001

This homework is intended to make you familiarize with Cadence schematic and symbol editor environment. Before you start this homework, make sure you finish all the steps in Cadence tutorial handouts.

1. Create parameterized inverter, nand2, nor2, xor2, and xnor2 gates schematic and symbol. You can use any circuit structure for xor2/xnor2 gates. (Create new library named "leafCells")

Submission: xor2 schematic plot, nand2 schematic/symbol plot

2. Draw 1-bit full-adder schematic with any combination of gates. You can also mix gates with transistors. An advanced VLSI student like you is responsible to use the proper transistor sizes. (Create new library names "Adder8")

Submission: 1-bit full-adder schematic and symbol plot

3. Draw 8-bit ripple-carry adder (RCA) using multiple-sheet schematic. Detailed description about multiple-sheet schematic can be found at

`http://www-scf.usc.edu/~ee577/tutorial/cadence_spr2000/cadence_tut2.pdf`

You will use two sheets and each of them will contain 4 full-adder cells. Inputs and outputs are named as

```
A[7:0], B[7:0], CIN: inputs
S[7:0], COUT: outputs
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Submission: 8-bit RCA schematic plot (2 sheet separately)

4. Create hspice netlist from 8-bit RCA schematic. Using hspice input deck, run hspice simulation and submit hspice simulation plot. Hspice input deck can be found at

`~ee577/ee577bb/hw/hw1.cir`

Submission: hspice simulation plot (S[7:0] and COUT)