PROLOGUE:

The first circuits course in an electrical engineering curriculum teaches that two fundamental laws govern the analysis of electrical networks. These two laws are the Kirchhoff Voltage Law (KVL), which is a manifestation of conservation of energy, and the Kirchhoff Current Law (KCL), which reflects conservation of charge. Without KVL and KCL, mathematical strategies that produce meaningful electrical characterizations of circuits cannot be formulated. The Kirchhoff laws reduce the art of circuit analysis to an engineering task whose conduct is rooted in basic physical principles.

Circuit analyses are conducted to understand the electrical behavior of circuits. Although KVL and KCL can be straightforwardly applied to even complicated circuits, understanding the engineering implications of the resultant equations is not a trivial task. Understanding does not always derive from mathematically precise solutions of KVL and KCL relationships. Indeed, closed form solutions may not be possible for certain classes of circuits unless approximations are invoked to simplify the analytical task. Even if exact closed form solutions can be found, their algebraic intricacy may obscure those circuit parameters that dominate circuit operating characteristics. Thus, the formulation and solution of the equilibrium equations for a circuit are not the objective of circuit analysis. Rather, the ultimate objective is to find circuit solutions—albeit approximate solutions—that illuminate salient circuit characteristics. Included among the tools, techniques, and theories that support this objective are superposition theory, the Thévenin and Norton equivalent circuits, Tellegen's theorem, the Laplace transform, and network phasors.

Circuit design is the task of producing manufacturable circuits whose electrical properties reliably satisfy requisite performance specifications. Because there is no analytical law that underlies a delineation of optimal topologies, circuit design is partially an art. But it is not exclusively an art, for a prerequisite to successful design is circuit understanding. If there is an implicit circuit design law, it is never to attempt to build a circuit that is not thoroughly understood.

The first step to circuit design is to recognize the type or types of circuits which show promise of realizing given operating requirements. Such cognizance is not possible without an analytical background that has addressed a broad variety of circuit types. Two reasons compel simplicity with respect to the choice of the first iteration design topology. First, topological simplicity promotes manufacturing ease, low cost producibility, and long term reliability. Second, the dynamics of simple circuit structures are easier to understand than are complicated networks. This understanding of the first design iteration is necessary to assess both its operating attributes and limitations. Circuit optimization, which leads to a progressively more complicated hierarchy of modifications to the first design iteration, is the result of ensuring that the electrical limits of performance associated with a design solution do not compromise requisite circuit performance for all realistic operating circumstances.

Insightful circuit analysis is the cornerstone of creative design. Without definitive analysis, the first step of the design process largely collapses to art, and without analysis, the propriety of subsequent circuit optimization is suspect. Accordingly, these notes set the stage for circuit and system design by reviewing the basic principles that govern a satisfying circuit analysis. Most importantly, they attempt to bolster student skills with respect to formulating analytical solutions that insightfully portray the engineering nature of circuit response dynamics.
1.1.0. CIRCUIT ELEMENTS

An electrical circuit is an array of electrical elements that are interconnected to allow for the flow of current. All electrical circuits are interconnections of only nine basic elements. Four of these elements—the ideal voltage source, the resistor, the capacitor, and the inductor—are commonly available two terminal components. They are physically realizable in that the measured volt ampere characteristics of their synthesized forms approximate the idealized mathematical relationships that define their respective electrical characteristics over wide operating ranges of voltages and currents.

A fifth element, the ideal current source, is a mathematical artifact that is often used to model the effect that a voltage source has on a circuit. Since it is a theoretic alternative to a voltage source, it is not available as an off the shelf component. Although an approximation of an ideal current source can be realized as a two terminal structure, the range of currents and voltages over which idealized current source behavior is closely achieved is more restrictive than the voltages and currents to which practical voltage sources, resistors, capacitors, and inductors can be subjected.

The final four elements encountered in electrical circuits are multi-terminal configurations. They are the ideal voltage amplifier, the ideal current amplifier, the ideal transconductance amplifier, and the ideal transresistance amplifier. Like the current source, none of these amplifying elements can be built to operate so that their defining volt ampere mathematics are emulated over wide ranges of voltages, currents, and frequency. They nonetheless satisfy an important engineering requirement. In particular, these four idealized elements can be used to simplify the electrical properties of complex amplifiers embedded in circuit topologies. They thus promote the mathematical tractability from which circuit understandability follows.

1.1.1. VOLTAGE SOURCE

The current flowing through a conductive element of a circuit is manifested by the transport of net charge through any cross section of the element. If \( i(t) \) represents the current in amperes that flows as a function of time \( t \) in seconds in response to the transport of net charge, \( q(t) \), in units of coulombs,

\[
i(t) = \frac{dq(t)}{dt}.
\]  

(1-1)

Without externally applied energy, intrinsic thermal agitation causes free charges to migrate randomly through a conductive element. Because this migration is random motion, the net average charge transported across any elemental cross section is zero, thereby resulting in a net average current of zero. In order to realize a non-zero average current, energy must be applied to the element to overcome thermally induced forces imposed on free charges. The vehicle for this requisite energy is generally a voltage source. With \( v(t) \) denoting the voltage corresponding to a net energy, \( w(t) \), required to direct the movement of a net charge, \( q(t) \), through an elemental cross section,
\[ v(t) = \frac{d w(t)}{d q(t)}, \]  

where \( v(t) \) has dimensions of volts when \( w(t) \) is in units of joules and \( q(t) \) is in coulombs.

Voltage sources are either time varying or time invariant. Examples of time varying ideal voltage sources, whose schematic representation is given in Fig. (1.1a), include sinusoids, step functions, periodic square waves, and impulse functions. Time invariant voltage sources are referred to as batteries or as power supplies. The schematic symbol of a time invariant voltage source is offered in Fig. (1.1b). From the graphical volt ampere characteristic curves accompanying these schematic diagrams, note that for both the time variant and time invariant cases, the current, \( i(t) \), flowing through an ideal voltage source is a constant, independent of the value of the voltage. It is important to understand that this current flows because the voltage source supplies energy to produce a directed motion of free charges in the element to which the voltage source is connected.

Fig. (1.1). (a). Schematic Symbol And Generalized Volt Ampere Characteristic Of A Time Varying Voltage Source. (b). Schematic Symbol And Volt Ampere Characteristic Of A Time Invariant Voltage Source
A measure of the amount of energy supplied to an element by an ideal voltage source is the power delivered by the voltage source. Power, \( p(t) \), is the time rate of change of energy. With \( v(t) \) and \( i(t) \) in disassociated reference polarity (current flowing from the minus end of the voltage source -to- the plus end), the power supplied to a conductive element by the voltage source diagrammed in Fig. (1.1a) is

\[
p(t) = \frac{dv(t)}{dt} = \frac{v(t) dq(t)}{dt} = v(t)i(t),
\]

where (1-1) and (1-2) are used. With \( v(t) \) in volts and \( i(t) \) in amperes, \( p(t) \) has dimensions of watts.

1.1.2. CURRENT SOURCE

The preceding section points out that a voltage source is the vehicle by which energy is imparted to free charges within a conductive element. If this energy is sufficiently large to overcome thermal energy that impacts all charges in conductive materials, a current flows through the conductive medium in accordance with (1-1). In effect, the voltage, say \( v(t) \), applied to a conductive element causes a current, \( i(t) \), to flow through the element, as suggested in Fig. (1.2a).

The foregoing cause and effect relationship between voltage and current can be reversed. In particular, energy delivered to charges within a two terminal conductive element can be viewed as the ramification of an applied ideal current source. If the current response, \( i(t) \), in Fig. (1.2a) is imagined as being generated by a source of constant current applied to the two terminal element in question, the applied current must result in the displacement of the same charge transported by the originally applied voltage source. Thus, the application of a current source of value \( i(t) \), as indicated in Fig. (1.2b), develops a voltage, \( v(t) \), across the terminals of the conductive element. The value of the developed voltage in Fig. (1.2b) is identical to that of the applied voltage in Fig. (1.2a).

Fig. (1.2c) offers the volt ampere characteristic of an ideal current source. Just as an ideal voltage source maintains a terminal voltage value that is independent of the current conducted by the voltage source, an ideal current source supplies a constant current that is invariant with the voltage developed across the current source.

1.1.3. RESISTOR

A resistor is a two terminal element whose voltage and current satisfy a prescribed algebraic relationship at any point in time\(^1\). Resistors are either nonlinear or linear, as abstracted Fig. (1.3). The nonlinear resistor depicted in Fig. (1.3a) has a volt ampere characteristic equation that can be written in either of the forms,

\[
v_R = f_R(i_R),
\]
or

\[ i_R = g_R(v_R) \]  \hspace{1cm} (1-5)

Fig. (1.2).  (a).  Current Flowing Through A Conductive Element In Response To A Voltage Applied Across The Element.  (b).  Voltage Developed Across A Conductive Element In Response To A Current Made To Flow Through The Element By Virtue Of The Application Of An Ideal Current Source.  (c).  Volt Ampere Characteristic Curve Of An Ideal, Constant Current Source.

Equations (1-4) and (1-5) apply at any instant of time, since neither of the functions, \( f_R(i_R) \) and \( g_R(v_R) \), depend on time derivatives or time integrals of current or voltage variables.

With the independent current variable, \( i_R \) in (1-4), expressed in units of amperes, the function, \( f_R(i_R) \) is in units of volts. Moreover, if \( f_R(i_R) \) is a single valued function of \( i_R \) (meaning that one and only one value of resistor terminal voltage corresponds to each and every value of current conducted by the resistor), the nonlinear resistor is termed a current controlled nonlinearity. Similarly, (1-5) is the favored mathematical form for a voltage controlled nonlinear resistance. If \( v_R \) is dimensioned in volts, \( g_R(v_R) \) has units of amperes. The characteristic curve plotted in Fig. (1.3a) indicates that the example nonlinear resistor is simultaneously a voltage controlled and
a current controlled element.

![Nonlinear Resistor Circuit Symbol](image)

**Fig. (1.3).** (a). Schematic Symbol And Generalized Volt Ampere Characteristic Of A Nonlinear Resistor. (b). Schematic Symbol And Volt Ampere Characteristic Of A Linear Resistor.

The generalized nonlinear resistor becomes a linear resistor if \( f_{R}(i_{R}) \) is a linear function of its independent current variable. Linearity reduces (1-4) to the Ohm's law relationship

\[
V_{R} = R i_{R},
\]

where \( R \), in units of ohms (V), is the resistance of the resistor. The applicability of (1-6) to a linear resistor demands that the current, \( i_{R} \), flowing through the element be in associated reference polarity with the voltage, \( V_{R} \), developed across the resistor. As suggested by the circuit schematic symbol of the linear resistor in Fig. (1.3b), this restriction means that \( i_{R} \) must flow from the plus side of \( V_{R} \) -to- the minus side of \( V_{R} \). An equivalent form of (1-6) is,
where \( G = \frac{1}{R} \) symbolizes the conductance of the resistance. The unit of conductance is the siemen (S) or the mho.

\[
i_R = 5 \frac{V_R}{R} - 5 G V_R, \tag{1-7}\]

Fig. (1.4). (a). Schematic Symbol And Generalized Volt Ampere Characteristic Of A Short Circuited Linear Resistor. (b). Schematic Symbol And Volt Ampere Characteristic Of An Open Circuited Linear Resistor.

There are two noteworthy special cases of a linear resistor. The first is the short circuit, which is defined as a linear resistor whose value of resistance, \( R \), is zero. For a short circuit, whose schematic representation and volt ampere characteristic curve are given in Fig. (1.4a), (1-6) confirms that the terminal voltage, \( V_R \), is zero, regardless of the current, \( i_R \), that flows through the element. A wire used to interconnect two components in an electronic circuit is a good approximation of a short circuit. It is an imperfect short circuit because no materials behave as ideal short circuits. In the case of a conductive wire, such as copper or aluminum, the resistance per unit length is an inverse function of the cross section area of the
wire. Thus, a "fat" length of copper wire is a better approximation of a short circuit than is a "skinny" copper wire of the same length.

The second special case is an open circuit. An open circuit is a linear resistor whose conductance, \( G \), is zero and whose corresponding resistance is therefore infinitely large. Equation (1-7) confirms that an open circuit maintains zero resistor current, \( i_R \), for all values of terminal voltage \( v_R \). Air and silicon dioxide comprise good examples of practical open circuits or, as they are commonly referred to, insulators. But just as there are no perfect short circuits, there are also no perfect insulators. For example, even air can conduct current at extreme voltage levels, as thunderbolts attest to during an intense electrical storm. Similarly, a thin layer of silicon dioxide, which often insulates metal from semiconductor surfaces in an integrated circuit, can break down and conduct current at high voltages. The schematic symbol and volt ampere characteristic curve of an open circuit are offered in Fig. (1.4b).

When energy is delivered to a resistor by a voltage or current source, as delineated in Fig. (1.5), the power associated with this energy delivery is dissipated as heat. This observation explains why a light bulb, which is an example of a nonlinear resistor, is hot to the touch shortly after it is energized. It also explains why a thin wire, which behaves as a linear resistor, is warm after it conducts large currents for a period of time.

In general, the power, \( p_R \), delivered to a resistor is the product of its voltage, \( v_R \), and corresponding current, \( i_R \), where \( v_R \) and \( i_R \) are in associated reference polarity. Thus, Ohm's law produces

\[
p_R = v_R i_R = i_R^2 R = v_R^2 G
\]

for a linear resistor. Observe that zero power is dissipated in either a short circuit \((R = 0)\) or an open circuit \((G = 0)\).

1.1.4. CAPACITOR

A capacitor stores charge as a function of the voltage impressed across its two terminals. Applied voltage is the engineering ramification of delivered energy. Since the charge stored on a capacitor is in one-to-one correspondence with the applied voltage and hence, with the energy delivered to it, a capacitor is an energy storage element. This energy storage function of a capacitor contrasts sharply with the electrical properties of a resistor. Rather than store energy, a resistor converts delivered energy into heat.

The circuit schematic symbol of a nonlinear capacitor is shown in Fig. (1.6a). With \( q_C \) denoting the charge stored on the capacitor and with \( v_C \) symbolizing the voltage applied to the terminals of the capacitor, the governing algebra for charge storage as a function of applied voltage is expressible as

\[
q_C = \mathcal{C} \left( v_C \right)
\]

(1-9)
where \( q_C \) is in units of coulombs when \( v_C \) is in volts. It follows from (1-1) that the current, \( i_C \), flowing through a capacitor is

\[
\frac{di_C}{dt} = 5 \frac{dq_C}{dt} = 5 \left[ \frac{df_C(v_C)}{dv_C} \right] \frac{dv_C}{dt} = 5 C(v_C) \frac{dv_C}{dt},
\]

(1-10)

where

\[
C(v_C) = \frac{df_C(v_C)}{dv_C},
\]

(1-11)

Fig. (1.5). (a). Energy Delivery To A Nonlinear Resistor By Either A Voltage Source Or A Current Source. (b). Energy Delivery To A Linear Resistor By Either A Voltage Source Or A Current Source.
representing the slope of the charge/voltage characteristic in Fig. (1.6a), is the effective capacitance of a capacitor that supports a voltage of $v_C$. For $f_{C}(v_C)$ in units of coulombs and $v_C$ in units of volts, the dimension of $C(v_C)$ is farads.

A linear capacitor, as diagrammed in Fig. (1.6b), has a charge function, $f_{C}(v_C)$, that is a linear function of the capacitor voltage, $v_C$. The resultant effective capacitance, $C(v_C)$ in (1-11), is a constant, say $C$, and (1-10) reduces to

\[ i = \frac{dQ}{dt} = C(v_C) \frac{dv_C}{dt}. \]  

Recall that the current flowing through a linear resistor is a linear function of the voltage applied across the resistor. On the other hand, the current that flows through a linear
capacitor is proportional to the time rate of change of the voltage applied to the capacitor. Off the shelf capacitive components having actual volt ampere characteristics that closely reflect (1-12) over wide ranges of voltages and currents are commonly available, especially when the value of the capacitance, \( C \), is no larger than a few microfarads (\( mF \)).

The linear capacitor is useful in analog active and passive filters and in digital memory cells. Ironically, the electrical properties that make capacitors useful in filtering, wave shaping, and information storage applications make them troublesome in others, such as high speed switching systems and wideband amplifiers. Most of the simultaneously interesting and troublesome characteristics of a linear capacitor stem from the fact that the current flowing through a capacitor is proportional, not to the voltage of capacitor voltage, but to the time rate of change of capacitor voltage. This means, for example, that a large capacitor voltage that is changing slowly with time incurs relatively small capacitive currents. Indeed constant voltages – albeit large constant voltages – make a capacitor behave as an open circuit, since (1-12) predicts \( i_C = 0 \) for constant \( v_C \). On the other hand, a small capacitor voltage changing rapidly causes large currents to flow through the element.

![Diagram](image)

**Fig. (1.7).** System Abstraction Of High Frequency Filtering Application Of A Linear Capacitor.

The fact that the current response of a linear capacitor is able to discriminate between slowly and rapidly varying input voltages makes it suitable for filtering applications. For example, suppose that a low frequency (slowly changing) input voltage to an electronic signal processor is contaminated by high frequency (rapidly changing) spurious signals, as abstracted in Fig. (1.7). Consider inserting a capacitor between ground and the node to which the signal processor output terminal and a load are incident. The impact of this capacitive filter is that the output currents generated by the high frequency input spurs are shunted to ground, thereby allowing the load to "see" only the currents produced by the low frequency input signal voltage that is to be processed. In effect, the capacitor isolates the load from the electrical effects of high frequency input contaminants.

But the foregoing example can also be used to illustrate an operational disadvantage. Suppose that the signal processor is to be designed so that both the low and the high frequency inputs are transmitted uniformly to the load. The capacitor in the diagram of Fig. (1.7) is now an undesirable element in that it inhibits high frequency current conduction through the load. The apparent engineering solution to this dilemma is the removal of the
subject capacitor. Unfortunately, shunt output capacitance is unavoidable. For example, the electrical nature of a physical load often implies intrinsic charge storage, and hence effective capacitance, across its terminals. Moreover, the interconnective wiring between the processor output terminal and the load is a potential problem because of the transported mobile charge associated with the current conducted by the wire. Since this charge is separated from the ground plane by an insulating dielectric (probably air or other type of insulator), the interconnect itself approximates a shunting capacitance that is continuously distributed along the length of the wire\[2].

The energy storage nature of a capacitor is likewise both an advantage and a disadvantage, depending on the application addressed. This contention is clarified by investigating the energy stored in a linear capacitor. If \( v_C(t) \) and \( i_C(t) \) respectively denote the time domain voltage developed across, and the current flowing through, a linear capacitor having capacitance \( C \), the power, \( p_C(t) \), delivered to the capacitor is

\[
p_C(t) = v_C(t) i_C(t) = C \frac{dv_C(t)}{dt}.
\]

Since the power, \( p_C(t) \), at time \( t \) is the time rate of change of the energy, \( w_C(t) \),

\[
dw_C(t) = C v_C(t) \frac{dv_C(t)}{dt}.
\]

An integration of this expression over a time interval of \( t \) to \( t_0 \) to any general time \( t \) leads to

\[
\int_{w_C(t_0)}^{w_C(t)} dw_C(x) = \int_{v_C(t_0)}^{v_C(t)} C v_C(x) dv_C(x),
\]

where \( x \) is a dummy variable. The resultant energy stored in the capacitor at time \( t \) is

\[
w_C(t) = \frac{1}{2} C v_C^2(t) = \frac{q_C^2(t)}{2C}, \quad (1-13)
\]

where use has been made of the fact that \( q_C(t) = C v_C(t) \) in a linear capacitor.

Equation (1-13) shows that the energy stored in a linear capacitor is in one-to-one correspondence with both the voltage applied across the capacitance and the charge stored within the element. It follows that arrays of capacitors can be used to store a variety of information, including numerical data and typed text. The only prerequisite underlying this electronic storage is that the information identified for archiving be appropriately encoded to voltages suitable for application across the terminals of the capacitive elements.

In addition to electronic data storage capabilities, linear capacitors can also remember stored data. A demonstration of this fact derives from a solution of (1-12) for the capacitor voltage, \( v_C(t) \), in terms of the capacitor current, \( i_C(t) \). To this end,
\[
dv C (t) = \frac{1}{C} \int_{t_0}^{t} i_C (x) \, dx.
\]

Upon integrating from time \( t = t_0 \) to any general time \( t \),
\[
\int_{t_0}^{t} \dv C (x) = \frac{1}{C} \int_{t_0}^{t} i_C (x) \, dx,
\]
whence
\[
v_C (t) = v_C (t_0) + \frac{1}{C} \int_{t_0}^{t} i_C (x) \, dx.
\]

Equation (1-14) defines, and Fig. (1.8) symbolically overviews, the voltage response, \( v_C(t) \), of a linear capacitor that is energized by a current, \( i_C(t) \), for time \( t > t_0 \). Unlike a resistor, this voltage response is not exclusively attributed to the applied current. Instead, \( v_C(t) \) is the superposition of two voltages. The first, \( v_C(t_0) \), is the voltage to which the capacitor is charged prior to the application of \( i_C(t) \), at \( t = t_0 \). This initial voltage, which corresponds to an initial charge, \( q_C(t_0) = Cv_C(t_0) \), stored in the capacitor at \( t = t_0 \) behaves as a battery in that it is a constant voltage, independent of current. If no current is conducted by the capacitor, the second term on the right hand side of (1-14) is zero, and the net instantaneous capacitor voltage is held fast at \( v_C(t_0) \) for all time. The second component of the net instantaneous capacitor voltage is the integral term on the right hand side of (1-14). This term is the voltage
that appears across the linear capacitor if said capacitor is uncharged at the instant of current application. In the course of responding to the applied current, $i_C(t)$, the capacitor therefore "remembers" the voltage ramification of charge stored on the capacitor prior to input current excitation. The time length of this memory can be very long, provided that $i_C(t)$ is zero or if $i_C(t)$ is very small and/or $C$ is very large.

The final noteworthy property of a linear capacitor is the reluctance of its terminal voltage to change quickly in the face of rapidly changing, finite currents. This property is a corollary to the memory feature discussed above; that is, a capacitor remembers its initial voltage immediately after a change in its current flow. It also reflects the fact that capacitor terminal voltage is in one-to-one correspondence with stored charge, which, when subjected to finite forces, cannot be transported instantly. The inability of a capacitor terminal voltage to change instantaneously can be confirmed analytically by solving (1-14) for the capacitor voltage, say $v_C(t_0l)$, immediately after initializing the flow of current, $i_C(t)$, through the capacitor at $t < t_0$. To this end, let $i_C(t)$ be bounded by an amplitude, $I_m$, for $t_0 < t < t_0l$; that is $|i_C(t)| < I_m$. Then

$$v_C(t_0l) < v_C(t_0) \frac{I_m}{C} \left[ \left( \frac{t_0l}{t_0} \right) - 2 \right].$$

(1-15)

Since the time difference, $(t_0l - t_0)$, is infinitesimally small, $v_C(t_0l) \approx v_C(t_0)$; that is, the capacitor voltage immediately after current excitation is identical to the capacitor voltage at the instant of a change in input current.

It is important to emphasize that instantaneous changes in capacitor voltages are precluded if and only if capacitor currents are finite. A result considerably different from $v_C(t_0l) \approx v_C(t_0)$ is obtained when the current flowing in a linear capacitor is impulsive. For example, let the capacitor current, $i_C(t)$, be the impulse function,

$$i_C(t) = \begin{cases} Q_m & t_0 < t < t_0l \\ 0 & \text{otherwise} \end{cases},$$

(1-16)

where $d(t_0l)$ signifies an impulse applied at time $t_0l$, and $Q_m$, a charge quantity, is the area enclosed by $i_C(t)$ in the time domain. Since $Q_m$ is a constant and $d(t_2t_0)$ encloses unity area for $t$. $t_0$, (1-14) gives

$$v_C(t) < v_C(t_0) \frac{Q_m}{C}.$$

(1-17)

Equation (1-17) confirms that a capacitor voltage at time $t$ can change instantaneously when an impulsive current excites the capacitor. In this case, the impulsive current adds a term, $Q_m/C$, to the initial voltage, $v_C(t_0)$, established immediately prior to the application of the impulse. In fact, the form of the voltage term generated by the impulsive current suggests that the charge, $Q_m$, associated with the input current is transferred directly to the capacitor. This observation
explains why engineering approximations of impulsive inputs are often used in the laboratory to investigate the zero input responses, which are the effects of initial conditions, of energy storage networks.

**EXAMPLE (1.1)**

The voltage waveform depicted in Fig. (1.9a) is applied across a 1.2 mF capacitor. Sketch the resultant time domain response of the current flowing through the capacitance. Assume that the capacitive current flows in associated reference polarity with the given voltage.

**SOLUTION (1.1)**

From (1-12), the current flowing through the capacitor is directly proportional to the time domain slope of the applied voltage signal. The constant of proportionality is the capacitance, \( C \), which is 1.2 mF.

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**Fig. (1.9).**

(a). Triangular Voltage Waveform Applied To The Linear Capacitor Addressed In EXAMPLE (1.1).

(b). Resultant Current Response Of The Voltage Waveform In (a). The Indicated Current Flows In Associated Reference Polarity With The Applied Voltage.
(1). For 0 mSEC, t, 6 mSEC, the time domain slope of the voltage waveform is constant, positive, and equal to 10 V/6 mSEC 5 1.667 kV/SEC. The resultant current is therefore constant and equal to C times this slope, or 2 mA.

(2). For 6 mSEC, t, 9 mSEC, the time domain slope of the voltage waveform is constant, negative, and equal to 210 V/3 mSEC 5 23.333 kV/SEC. The resultant current is therefore constant and equal to C times this slope, or 24 mA.

(3). In the time interval, 9 mSEC, t, 15 mSEC, the time domain slope of the voltage waveform is zero. The resultant current is likewise 0.

(4). The second triangular pulse in the waveform of Fig. (1.9a) replicates the first pulse, whose effects have just been studied. Accordingly, the resultant capacitive current, flowing in associated reference polarity with the applied voltage, is as depicted in Fig. (1.9b).

Note that the effect of the capacitor is to produce a current waveform whose time domain shape differs considerably from that of the applied voltage signal. This problem therefore suggests that capacitors have utility in wave shaping applications.

**EXAMPLE (1.2)**

The current waveform depicted in Fig. (1.10a) flows through a 1.2 mF capacitor. Sketch the resultant time domain response of the voltage developed across the terminals of the capacitance, assuming that the capacitor voltage, v_C(t), is zero at time t 5 0. Assume that the given current flows in associated reference polarity with the capacitor voltage.

**SOLUTION (1.2)**

Equation (1.14) is the relevant expression for computing the voltage developed across the terminals of the subject capacitor.

(1). For 0 mSEC < t < 6 mSEC, the current, i_C(t), flowing through the capacitor is a constant value of 1 mA. Since v_C(0) is given as zero, the capacitor voltage in the indicated time interval is

\[
v_C(t) = \frac{1}{(1.2)(10^{-6})} \int_0^t (1)(10^{2.3}) \, dx = \frac{t}{12},
\]

where t in mSEC delivers v_C(t) in volts. Clearly, v_C(t) is linear with time, and v_C(6) 5 5 volts.

(2). For 6 mSEC < t < 15 mSEC, zero current flows through the capacitor.
From (1-14), the five volts to which the capacitor charged during the first time interval addressed in the preceding step is resultantly sustained throughout the 6 mSEC -to- 15 mSEC interval; that is \( v_C(t) = 5 \) volts.

(3). In the time interval, 15 mSEC < \( t < 21 \) mSEC, the capacitor current reverts to \( i_C(t) = 1 \) mA, a constant. Unlike the 0 mSEC -to- 6 mSEC interval, the capacitor voltage is 5 volts at the start of the second 1 mA pulse. Using (1-14) once again, the resultant capacitor voltage for 15 mSEC < \( t < 21 \) mSEC is

\[
v_C(t) = 5 + \frac{1}{(12)} \int_{15}^{t} (1) \, dx = 5 + \frac{t - 15}{12},
\]

where \( t \) in mSEC gives \( v_C(t) \) in volts. Observe that \( v_C(21) = 10 \) volts, and since \( i_C(t) = 0 \) for \( t > 21 \) mSEC, \( v_C(t) = 10 \) volts for all time \( t > 21 \) mSEC. The resultant capacitor voltage, developed in associated reference polarity with the current flowing through the capacitor, is portrayed in Fig. (1.10b).
The effect of the capacitor is to produce a current waveform whose time domain shape differs considerably from that of the applied voltage signal.

1.1.5. **INDUCTOR**

In addition to implying a directed mobility of electrical charge, a current flowing through a conductive element sets up a magnetic field\[^3\]. The flux, $f_L$, of this magnetic field is generally a nonlinear function of the current, $i_L$, in accordance with the algebraic relationship,

$$ f_L = f_L(i_L). $$  \hspace{1cm} (1-18)

If the flux is a linear function of the current, (1-18) reduces to
\[ f_L = L \frac{d}{dt} i_L, \] (1-19)

and the element in question is known as a linear inductor. The parameter, \( L \), in this equation is called the inductance of the inductor. With \( f_L \) in units of webers and \( i_L \) dimensioned in amperes, \( L \) has units of henries.

By Faraday's Law, a time varying current flowing through an inductor induces an inductor terminal voltage that is the time rate of change of magnetic flux. For the linear inductor, whose circuit schematic representation is given in Fig. (1.11), this terminal voltage, say \( v_L \), is

\[
   v_L = \frac{df_L}{dt} = L \frac{di_L}{dt},
\]  

(1-20)

where voltage \( v_L \) and current \( i_L \) are in associated reference polarity. A comparison of (1-20) with (1-12) suggests a volt ampere duality between the capacitor and the inductor; that is, the mathematical form of (1-20) is identical to that (1-12), save for an interchange of voltage and current variables. Thus, the electrical properties of an inductor can be inferred from the corresponding electrical properties of a capacitor.

Energy can be stored by a capacitor in the form of stored charge. Energy can likewise be stored in the magnetic flux associated with the current flowing in an inductor. The amount, \( w_L(t) \), of this stored energy is

\[
   w_L(t) = \frac{1}{2} L i_L^2(t) = \frac{f_L^2(t)}{2L}.
\]  

(1-21)

The energy stored in the magnetic flux of a linear inductor is seen to be in one-to-one correspondence with both the magnetic flux and the inductor current that establishes the flux. Inductors can therefore be used as data storage elements, provided that the data identified for storage is encoded to a current suitable for conduction by an inductor. However, there is no widespread use of inductors as data storage elements because of inherent difficulties associated with the manufacturing of small two terminal components whose electrical characteristics approximate those of linear inductors.
(2). The inductive counterpart to (1-14) is the current relationship,

$$i_L(t) = i_L(t_0) + \frac{1}{L} \int_{t_0}^{t} v_L(x) \, dx,$$

which shows that an inductor "remembers" stored information in the form of an initial current, $i_L(t_0)$. The electrical implication of (1-22) is highlighted by the circuit of Fig. (1.12a). At time $t = t_0$, switch $S_1$ is thrown to connect node "B" to "E" and simultaneously, switch $S_2$ is thrown to interconnect nodes "C" and "D." Immediately before time $t_0$, $S_1$ connects node "A" to node "B," and $S_2$ interconnects node "A" with node "D," thereby effecting a current, $i_L(t_0)$, flowing through the inductor of inductance value $L$. When the two switches are thrown at $t > t_0$, this current initializes the net instantaneous inductor current, $i_L(t)$, for $t > t_0$. The result is that the circuit given in Fig. (1.12b) models the circuit in Fig. (1.12a) for $t > t_0$.

(3). Recall that the voltage across a capacitor excited by finite current cannot be made to change instantaneously. For the case of an inductor, current cannot change instantaneously, as long as the time domain voltage across the terminals of the inductor is finite. Impulsive inductor terminal voltages do produce instantaneous changes in current, just as impulsive currents flowing through capacitors permit instantaneous changes in capacitor voltages.

Although inductive components are seldom used in microelectronics, they play a pivotal role in explaining parasitic coupling phenomena in electronic circuits and systems. Undesirable electrical coupling between two conductive and adjacent circuit paths is often the cause of excessive distortion, electrical interference, and even dynamical instability. An example of spurious coupling is the audio and video noise evidenced in a television receiver operated near a heavy duty power tool. In the absence of sufficient shielding between the television antenna lead in wire and the power cord of the electrical tool, magnetic fields precipitated by the relatively large currents conducted by the tool can envelop, or couple with, the antenna lead in cable. Since appliances are powered by sinusoidal currents, the flux produced by the power tool changes with time, thereby inducing voltages along incremental lengths of both the appliance power cord and the antenna cable. The result is that the net effective signal established across the antenna input terminals of the television receiver is due to both the transmitted signal received by the antenna and coupled voltages induced by the current that energizes the power tool. The upshot of this undesired coupling is impaired audio and/or visual reception. To be sure, the magnetic fields of the antenna cable also couple with those of the power cord of the tool. However, the fields produced by the very small antenna currents induce proportionately small voltages across incremental lengths of the power cord of the tool and therefore, they exert an almost immeasurable influence on the electrical performance of the tool.
A more subtle, but nonetheless potentially troublesome, version of the foregoing scenario prevails in integrated circuits designed to process high frequency input signals. A time varying current made to flow through one signal path of this circuit creates a magnetic flux that induces a voltage, in concert with (1-20), along the path. But the same flux field can wrap around a second conductive path laid out in close proximity to the first. Accordingly, a voltage is induced in the second path, as well as in the first, thereby implying that the signal flow properties of the second path are not determined exclusively by the excitations and electrical elements indigenous to that path. Suppose that the perturbed second conductive path comprises the dominant artery for the transmission of high frequency input signals from the input port –to– the output port of a wideband integrated circuit. If the parasitically coupled signal is polarized in such a way as to oppose the flow of high frequency signals, bandwidth deterioration results. Yet another possible problem surfaces if the perturbed signal path is part of a feedback loop. In this case, the coupled signal may produce excessive time delays that can lead to unsatisfactory stability margins or even instability, in the sense of spurious oscillations over certain frequency ranges.

1.1.6. DEPENDENT SOURCES

The voltage source, current source, resistor, capacitor, and inductor overviewed in the preceding sections are all two terminal elements that commonly appear as single branches in electrical and electronic circuits. In contrast, the final four circuit elements –the ideal voltage amplifier, the ideal current amplifier, the ideal transconductance amplifier, and the ideal transresistance amplifier– are dual branch circuit elements having at least three, and often four, terminals. Each of these idealized amplifiers are modeled by a voltage or a current source placed in a branch that is termed the controlled branch. The value of the controlled...
voltage or current source is exclusively dependent on a current flowing through, or on a voltage developed across, a second circuit branch that is referred to as the controlling branch. Collectively, the controlled and controlling branches comprise a dependent source. The volt ampere characteristics of a dependent voltage or a dependent current source are a first order circuit level ramification of complex physical processes taking place in electrical, electronic, mechanical, electro-mechanical, or other types of systems undergoing analysis. The four dependent sources described below are ideal in the sense that all of these sources lack internal resistances, capacitances, and inductances.

1.1.6.1. IDEAL VOLTAGE AMPLIFIER

An ideal voltage amplifier delivers a voltage across its controlled branch that is proportional to the controlling branch voltage established by independent sources of excitation. The dependent source used to model the electrical properties of this type of amplifier is a voltage controlled voltage source (VCVS). Its schematic representation is offered in Fig. (1.13), for which the characteristic volt ampere equations are

\[
\begin{align*}
    &i_i = 0 \\
    &v_o = m v_i
\end{align*}
\]

(1-23)

In (1-23), \(i_i\) is a null input current flowing in the open circuited controlling branch of the source, \(v_i\) is the voltage across the controlling branch, \(v_o\) is the voltage appearing across the controlled branch, and \(m\) is a voltage amplification factor, or voltage gain. The controlled voltage of a VCVS remains \(m v_i\), regardless of any resistive, capacitive, or inductive load placed across the terminals of the controlled branch.

A VCVS is commonly invoked to model the low frequency transfer characteristics of an operational amplifier (op-amp). The circuit schematic diagram of Fig. (1.14a) portrays an op-amp as a five terminal device. Constant voltages, \(V_{CC}\) and \(V_{EE}\), which are known as biasing voltages, are applied to two of the five op-amp terminals to achieve nominally linear input-to-output transfer characteristics. In the schematic diagram, it is understood that the negative terminal of the \(V_{CC}\) source lies at ground potential, as does the positive terminal of the \(V_{EE}\) bias supply. Input signal voltages are applied to either or both of the terminals labeled as (2) and (1), which are respectively referred to as the inverting and the non-inverting input ports. As a result of applied input signals, a differential voltage, \(v_d\), is developed from the inverting input terminal -to- the non-inverting input port. In response to the non-zero differential input voltage, \(v_d\), a single ended output voltage, \(v_o\), is generated from the output terminal of the op-amp -to- ground.

In an ideal operational amplifier, the two input currents, \(i_2\) and \(i_1\), are zero. Moreover, the relationship of \(v_o\) to \(v_d\) is as depicted graphically in Fig. (1.14b). Over the
Fig. (1.13). Schematic Diagram Of A Voltage Controlled Voltage Source (VCVS) Used To Model The Volt Ampere Characteristics Of An Ideal Voltage Amplifier.

output voltage range, $2V_{EE} < v_o < 1V_{CC}$, this relationship is linear and expressible as

$$v_o = 2A_{OL}v_d,$$

(1-24)

where $A_{OL}$ is termed the open loop gain of the op-amp. This simple linear relationship and the fact that $i_2 = i_1$ allow the ideal op-amp to be modeled by a VCVS, as shown in Fig. (1.14c). It is important to note that the VCVS model of an op-amp is valid only for output signal voltage excursions of $2V_{EE} < v_o < 1V_{CC}$. From (1-24), this output signal range corresponds to a differential input signal swing of

$$2 \frac{V_{CC}}{A_{OL}} < v_d < 1 \frac{V_{EE}}{A_{OL}}.$$  

(1-25)

A practical op-amp, has $A_{OL}$ of the order of tens-to-even hundreds of thousands. Thus, (1-25) imposes severe restrictions on the allowable input signal swing. For example, in an op-amp having $A_{OL} = 80,000$ and biased with $V_{CC} = V_{EE} = 12$ volts, linearity requires that the differential input voltage be restricted to the range $-v_d < 150$ mvolts!

![Diagram](attachment:image1.png)

(a).

![Diagram](attachment:image2.png)

(b).
A second example of the use of a VCVS is the analysis of active RC filters. Consider the low pass filter of Fig. (1.15a)\cite{4}. This structure uses an amplifier having a voltage gain, \( k \), which means that for a suitable range of input voltages, \( v_x, v_o \approx k v_x \). Assuming that the amplifier draws no input current, \( (i_x = 0) \) a useful equivalent circuit of the filter is the VCVS topology depicted in Fig. (1.15b).

### 1.1.6.2. Ideal Current Amplifier

The ideal current amplifier is the dual of the ideal voltage amplifier. More specifically, an ideal current amplifier produces a current flowing through its controlled branch that is proportional to the controlling branch current established by independent sources. The dependent source used to model the electrical properties of a current amplifier is a current controlled current source (CCCS). Its schematic representation in Fig. (1.16), suggests characteristic volt ampere equations of the form,

\[
\begin{align*}
&v_1 i_1 = 0 \\
&i_o = b i_1
\end{align*}
\]

where \( b \) is termed the current gain of the CCCS. Note that \( v_1 \) is the null input voltage across the controlling branch of the CCCS, \( i_1 \) is the input current flowing through the short circuited controlling branch, and \( i_o \) designates the output current conducted by the controlled branch. The output current remains \( b i_1 \), regardless of the electrical nature of any load connected across the two terminals of the controlled branch.

Under certain operating conditions, a bipolar junction transistor (BJT) behaves as a current controlled current source. The BJT is a three terminal device, as indicated by its circuit schematic symbol in Fig. (1.17). These terminals are the collector (C), base (B), and emitter (E). The controlled, or output, current, \( i_c \), flows into the collector. To first order, the collector
current is proportional to the controlling, or input, current, $i_b$, by a factor of a constant, $h_{FE}$; that is,

$$i_c = h_{FE} i_b.$$  \hspace{1cm} (1-27)

As is substantiated later in this text, the approximate equivalent circuit of a BJT, which capitalizes on the CCCS nature of (1-27), is the structure depicted in Fig. (1.18). The battery of voltage $V_E$, which appears in series with the base terminal, reflects the electrical impact of physical processes intrinsic to the transistor.

1.1.6.3  \hspace{0.2cm} IDEAL TRANSCONDUCTANCE AMPLIFIER

As is the case with an ideal current amplifier, the controlled variable of an ideal transconductance amplifier is a current that is independent of any electrical load imposed across the terminals of the controlled branch. But unlike the current amplifier, the controlled current of a transconductance amplifier is linearly proportional to the voltage appearing across the open circuit terminals of the controlling branch.

The dependent source pertinent to a transconductance amplifier is a voltage controlled current source (VCCS). Its schematic representation appears in Fig. (1.19), for which the volt ampere relationships are
where \( g_m \) is the transconductance of the VCCS. The current, \( i_i \), is the null input current flowing in the controlling branch of the VCCS, \( v_i \) is the voltage developed across the terminals of the open circuited controlling branch, and \( i_o \) is the output current in the controlled branch.

There are several active semiconductor devices which, when operated under restricted voltage and current conditions, have transfer characteristics that approximate those of the VCCS. Among these devices are the vacuum tube, the junction field effect transistor (JFET), the metal oxide semiconductor field effect transistor (MOSFET), and the gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET). Even a circuit realized in bipolar technology can be made to behave nominally as a voltage controlled current source.

Consider, for example a type of MOSFET known as an N channel MOSFET, whose schematic symbol is provided in Fig. (1.20a). The three terminals of a MOSFET are known as the drain (D), the gate (G), and the source (S). The controlled current is the drain current, \( i_d \).
and the voltage appearing across the controlled port is the drain-source voltage, $v_{ds}$, as indicated in the figure. The gate-source voltage, $v_{gs}$, serves as the controlling variable, whence

$$i_d = g_m v_{gs}.$$  

(1-29)

The resultant first order MOSFET equivalent circuit, which is explored thoroughly in later chapters, is the VCCS topology submitted in Fig. (1.20b).

1.1.6.4. **IDEAL TRANSRESISTANCE AMPLIFIER**

Just as the current amplifier is the dual of the voltage amplifier, the ideal transresistance amplifier is the dual of the transconductance amplifier. The transresistance configuration is modeled by a current controlled voltage source (CCVS). As shown in Fig. (1.21), the relevant characteristic equations are

$$\begin{align*}
  v_i &= 0 \\
  v_o &= r_m i_i
\end{align*}$$

which typifies the fact the controlled variable, $v_o$, of a CCVS is a voltage that is linearly dependent on the input current, $i_i$, flowing through the short circuited terminals of the controlling branch. The controlled voltage of a CCVS is invariant with the electrical characteristics of loads incident with the output terminals of its controlled port. The parameter, $r_m$, is termed a transresistance.

![Fig. (1.21). Schematic Diagram Of A Current Controlled Voltage Source (CCVS) Used To Model The Volt-Ampere Characteristics Of An Ideal Transresistance Amplifier.](image)

1.2.0. **KIRCHHOFF'S LAWS**

At this juncture, a circuit has been defined as a conductive, interconnected array of elements. Additionally, the mathematics underlying the volt ampere characteristics of the nine fundamental elements of an electrical circuit have been explored. This backdrop leads naturally to a review of circuit analysis methods, whose goal is to promote an understanding
of the interrelationships among the volt ampere characteristics of circuit elements, the topological structure of the interconnection of these elements, and the resultant input -to-output (I/O) circuit relationships.

Circuit analysis formalizes a set of independent equations whose simultaneous solution yields the currents flowing through, and the corresponding voltages appearing across, all circuit elements. The relevant analytical tools are the Kirchhoff Current Law (KCL) and the Kirchhoff Voltage Law (KVL), which are the circuit level ramifications of conservation of charge and conservation of energy, respectively. A systematic application of KCL and KVL to generalized circuit structures requires an understanding of a few concepts related to the topology of circuits; that is, the interconnective structure of the elements embedded in the circuit.

1.2.1. TOPOLOGICAL CONCEPTS

The circuit branch is the first of the topological concepts to which the preceding section of material alludes. A branch of a circuit is any two terminal circuit element. Thus, circuits have independent voltage and current source branches, resistor branches, capacitor branches, inductor branches, and branches that define the controlling or controlled terminal pairs of any one of the four possible dependent sources. The terms, element and branch, and the phrases, branch element and circuit branch, as applied to electrical circuits, refer to the same thing. The circuit abstracted in Fig. (1.22) displays seven branches, which are labeled b1 - through- b7. Since this circuit is drawn without a delineation of the specific electrical nature of each of the seven branches, the circuit displays only the topology of the network.

The interconnection of precisely two branches of a circuit is a junction. On the other hand, the interconnection of two or more circuit branches comprises a circuit node. A junction is therefore a special case of a node. The circuit of Fig. (1.22) has five nodes; these are numbered 0 -through- 4. Only node 1, which interconnects branches b1 and b2, is a junction.

If at least one branch of a circuit is an independent voltage or current source, current can be expected to flow through all circuit branches. Since the true direction in which these currents flow is unknown prior to an actual circuit analysis, it is necessary to assume a positive current direction for each and every circuit branch. In general, the polarity direction of B such currents must be assumed for a circuit containing B branches. In associated reference polarity correspondence to each of the B branch currents in a B branch circuit, there are B branch voltages. The branch currents and voltages for the circuit of Fig. (1.22) are symbolized as i1 -through- i7 and v1 -through- v7, respectively. It is important to underscore the fact that while the choice of the branch current directions in any circuit is arbitrary, the selected polarities of the branch voltages is not vagarious. In particular, once a reference direction for each branch current is chosen -albeit chosen arbitrarily- the associated reference polarity convention dictates the polarity of each corresponding branch voltage.
A loop of a circuit is a collection of branch elements that collectively comprise a closed path. Practical circuits have numerous loops. Three loops of the circuit in Fig. (1.22) are the sequence of branches, b11b21b31b5, b71b61b51b3, and b11b21b31b41b6. A loop is independent of the assumed positive reference directions of branch currents and voltages, and it is also independent of the branch sequence adopted to define the loop. Thus, the loop, b11b21b31b5, is identical to the loop defined by b51b21b11b3.

A mesh is a special case of a loop in that it is a loop that encloses or encircles no branch of the circuit. A circuit having B branches and (N/1) nodes, has (B2N) meshes. The number, say M, of meshes in the circuit of Fig. (1.22) is three, since the circuit at hand has N54 and B57. These meshes are easily identified as the branch sequences, b11b21b31b5, b31b41b7, and b41b61b5.
Fig. (1.23). (a) Circuit Of Fig. (1.22) Drawn To Indicate The Four Circuit Node Voltages. (b) Simplified Version Of (a). The Ground Node Is Node 0.
The node voltages of a circuit are the voltages, measured with respect to a common reference node, that are developed at each circuit node. In an \((N/1)\) node circuit, there are \((N/1)\) definable node voltages. But since one circuit node serves as the reference point for all circuit node voltages, the voltage of the reference node is defined to be zero. There are therefore only \(N\) computable node voltages in an \((N/1)\) node circuit. In Fig. (1.23a), these computable voltages are indicated as \(e_1\) through \(e_4\), where node 0 is assumed to be the reference node. The reference node adopted in a circuit analysis problem is indicated by the ground symbol, which serves as the reference, or "2" end of each circuit node voltage, as shown in Fig. (1.23b).

1.2.2. KIRCHHOFF CURRENT LAW

The Kirchhoff Current Law (KCL) states that at any time, the algebraic sum of currents at each node of a circuit must be zero. Equivalently, KCL asserts that the net sum of currents that enter a node must be identical to the net sum of currents that leave the same node. KCL reflects charge conservation principles; that is, charge can neither be destroyed nor created during its transport across an arbitrary cross section of a conductive element.

The maximum number of independent KCL equations that can be written for an \((N/1)\) node, \(B\) branch circuit is \(N\). Recall that in an \((N/1)\) node circuit, only \(N\) node voltages can be computed. This observation leads to the suspicion that the objective of KCL analysis, or nodal analysis, as it is commonly referred to, is a unique solution for the \(N\) computable node voltages of an \((N/1)\) node circuit.

Four preliminary tasks are conducted, usually by inspection, prior to a systematic application of KCL. First, the reference node, the \(N\) remaining nodes of an \((N/1)\) node circuit, and the \(B\) branches of the circuit are identified. Second, branch currents are assigned symbolically to each of the \(B\) circuit branches, and a positive direction is assumed for each of these branch currents. Recall that the direction in which positive current flows is arbitrary. But in concert with the associated reference polarity convention, the polarity of branch voltages derives directly from the assumed directions of corresponding branch currents.

The third preliminary task stems from the fact that the application of KCL involves an algebraic sum of nodal currents. This means that at each circuit node, a decision must be made as to whether to view a current entering a node as a positive or a negative variable. If an entering nodal current is viewed as a positive circuit variable, a current leaving the same node is necessarily a negative variable, and vice versa. The algebraic sign convention adopted at a node is arbitrary, and it need not be consistent from node-to-node. In other words, currents perceived as positive quantities when they leave one circuit node can be taken as negative variables when they leave another circuit node. However, to minimize confusion and to achieve a systematic analytical tack, the algebraic sign convention adopted for currents at a particular circuit node is uniformly enforced at all nodes.

Finally, since a nodal analysis leading to an independent set of KCL relationships requires that KCL be applied to only \(N\) of the \((N/1)\) circuit nodes, \(N\) specific nodes must be earmarked for KCL analysis. In practice, KCL is not explicitly invoked at the reference or...
ground node of the circuit undergoing analysis.

For the circuit of Fig. (1.23b), KCL, applied at nodes 1 -through- 4 in such a way that currents leaving a node are viewed as positive electrical variables, yields

\[
\begin{align*}
\text{node #1:} & \quad 0 & 5 & 2i_1 & i_2 \\
\text{node #2:} & \quad 0 & 5 & 2i_1 & i_1 & i_7 \\
\text{node #3:} & \quad 0 & 5 & 2i_2 & i_1 & i_2 & i_5 \\
\text{node #4:} & \quad 0 & 5 & i_4 & i_5 & i_7 \\
\end{align*}
\]

(1-31)

For sake of completeness, a similar nodal analysis at node 0 gives

\[
\begin{align*}
\text{node #0:} & \quad 0 & 5 & i_1 & i_2 & 2i_6. \\
\end{align*}
\]

(1-32)

But this equation is not independent of (1-31) since (1-32) is the negative sum of the four KCL relationships in (1-31). Actually, any four of the five expressions collectively implicit to (1-31) and (1-32) comprise an independent set of KCL equations. To confirm an earlier contention that the algebraic sign convention adopted for the branch currents at a particular circuit node need not be uniformly applied to all circuit nodes, reconsider node 3 in the circuit of Fig. (1.23b). This time, let currents be defined as positive when they enter, as opposed to leave, node 3. Then KCL gives

\[
\begin{align*}
\text{node #3:} & \quad 0 & 5 & i_3 & i_4 & i_5, \\
\end{align*}
\]

(1-33)

which is tantamount to multiplying both sides of the third KCL expression in (1-31) by (21).

1.2.3. KIRCHHOFF VOLTAGE LAW

The Kirchhoff Voltage Law (KVL) states that at any time, the algebraic sum of voltages around all loops of a circuit must be zero. KVL reflects conservation of energy; that is, energy can neither be destroyed nor created. Instead, the energy applied to a circuit loop can only be stored in the electrostatic charge fields of capacitive branch elements, it can be stored in the magnetic flux fields associated with inductor branches, or it can be dissipated as heat in resistive circuit branches.

The maximum number of independent KVL equations that can be written for an (N/1) node, B branch circuit is (B2N). Since (B2N) is the number of meshes in an (N/1) node, B branch circuit, a systematic KVL analysis is accomplished by writing KVL equations for only circuit meshes. The objective of KVL analysis, which is otherwise known as loop analysis or mesh analysis, is a unique solution for (B2N) circuit mesh currents.

As in the case of KCL, four simple tasks are conducted in advance of an application of KVL. First, the reference node, the N remaining nodes of an (N/1) node circuit, and the B branches of the circuit are identified. Second, branch currents are assigned symbolically to
each of the \( B \) circuit branches, and a positive direction is assumed for each of these branch currents. By the associated reference polarity convention, the polarity of branch voltages derives directly from the assumed directions of corresponding branch currents.

The third task involves a choice of mesh (or loop) orientation. In particular, KVL can be applied by adding branch voltages encountered in either a clockwise or a counterclockwise analytical "walk" around each mesh. Loop orientations can differ from loop-to-loop, but consistency in the adoption of an orientation is advised. A related final task is the adoption of a convention in regard to positive and negative branch voltages within a mesh. For an adopted loop orientation, a branch voltage is considered positive when the positive terminal of the branch voltage is encountered before the negative terminal. Like the loop orientation, this convention is also arbitrary and can be changed from loop-to-loop.

The circuit in Fig. (1.23b) has five nodes and seven branch elements. Accordingly, \( N = 4 \), \( B = 7 \), and \( M \), the number of circuit meshes, is \( M = (B-N)/2 = 3 \). As discussed earlier, these three meshes are defined by the branch sets, \( b_{11}b_{12}b_{13}b_{15} \), \( b_{31}b_{41}b_{7} \), and \( b_{41}b_{61}b_{5} \). The pertinent KVL equations are

\[
\begin{bmatrix}
0 & 5 & 1 & v_1 & 1 & v_2 & 1 & v_3 & 2 & v_5 \\
0 & 5 & 1 & v_3 & 2 & v_4 & 1 & v_7 \\
0 & 5 & 2 & v_4 & 1 & v_6 & 1 & v_5 \\
\end{bmatrix}
= 0.
\]

(1-34)

1.2.4. CONSERVATION OF POWER

The Kirchhoff Current Law and the Kirchhoff Voltage Law ensure that electrical circuits conserve charge and energy. But additionally, circuits conserve power. To expand on this contention, consider the \( k \)th branch of a \( B \) branch electrical circuit, as depicted in Fig. (1.24). The power delivered to this \( k \)th branch is the product, \( v_ki_k \), of the voltage, \( v_k \), developed across the \( k \)th branch and the current, \( i_k \), flowing through the branch. Note that the electrical variables, \( v_k \) and \( i_k \), are in the associated reference polarity convention. Tellegen’s theorem asserts that if the \( B \) values of \( v_k \) and the \( B \) values of \( i_k \) satisfy KVL and KCL, respectively, the algebraic sum of all such powers delivered to each of the \( B \) circuit branches is zero \([5]\); that is,

\[
\sum_{k=1}^{B} v_k i_k = 0.
\]

(1-35)
The satisfaction of (1-35) demands that at least one of the product terms, \( v_{kik} \), be negative. Since \( v_{kik} \) represents the power delivered to the \( k \)th branch, \( v_{kik} > 0 \) indicates that the energy associated with this power is either stored in the \( k \)th branch or dissipated by the \( k \)th branch as heat. It follows that, \( v_{kik} < 0 \) suggests that the \( k \)th branch is generating power or equivalently, the \( k \)th branch is delivering energy to the rest of the circuit. If there are \( S \) branches, numbered 1 -through- \( S \) for convenience, for which \( v_{kik} < 0 \) the net power, \( p_{in} \), applied to an electrical circuit is

\[
p_{in} = \sum_{k=1}^{S} v_{kik} i_k,
\]

(1-36)

where \( p_{in} \) is understood to be non-negative. The remaining \((B - S)\) branches are characterized by \( v_{kik} > 0 \), and thus, they either store energy or dissipate power. If \( p_{dis} \) designates the \((B - S)\) term sum for which the delivered branch powers are actually positive,

\[
p_{dis} = \sum_{k=S+1}^{B} v_{kik} i_k,
\]

(1-37)

Equations (1-37) and (1-36) reduce (1-35) to

\[
p_{in} = p_{dis},
\]

(1-38)

where both \( p_{in} \) and \( p_{dis} \) are non-negative power terms.

Equations (1-35) and (1-38) provide a relatively convenient means of checking the computational propriety of the branch voltages and branch currents deduced from an application of KVL and/or KCL. In particular, computational errors are assured if the \( v_k \) and \( i_k \) evaluated for all \( B \) branches of a given network do not satisfy (1-35). Moreover, (1-35), and particularly (1-38), are routinely exploited as a first level laboratory test to screen out faulty integrated circuits. Because limiting the net average power dissipated, \( p_{dis} \), by an electronic circuit is an important design requirement, the average power consumed by each branch implicit to the circuit is invariably calculated. By (1-37), the sum of these branch power terms is the net power, \( p_{dis} \), consumed by the entire circuit. But since the branches intrinsic to a fabricated integrated circuit are not straightforwardly accessible for test and evaluation, the net power consumed by the circuit is measured indirectly by measuring the power supplied, \( p_{in} \), to the circuit by requisite sources of external energy. A possible design or manufacturing problem is indicated whenever the measured \( p_{in} \) differs substantially from the calculated \( p_{dis} \).
EXAMPLE (13)

Use mesh and nodal analyses to solve for all branch currents and all node voltages in the circuit given in Fig. (1.25). The parameters of the circuit are as follows:

\[
\begin{align*}
R_1 & = 5 \text{ } 10 \text{ V} & R_2 & = 5 \text{ } 100 \text{ V} \\
R_3 & = 5 \text{ } 15 \text{ V} & R_2 & = 5 \text{ } 600 \text{ V} \\
R_5 & = 5 \text{ } 2,000 \text{ V} & E & = 5 \text{ } 12 \text{ volts}.
\end{align*}
\]

SOLUTION (13)

The circuit at hand has five resistive branches and one voltage source branch for a net total of six circuit branches. Aside from ground, there are three other circuit nodes, whose node voltages (referenced to ground) are symbolized as \(E_1\), \(E_2\), and \(E_3\). With \(B = 6\) and \((N/1) = 4\), the number of circuit meshes is \(M = 3\).

1. Three mesh equations are required to solve an independent set of KVL equations for the circuit. To this end, let the current flowing through resistor \(R_1\) be \(I_1\), and let the currents conducted by resistors \(R_3\) and \(R_5\) be \(I_2\) and \(I_3\), respectively. An application of KCL to the third node indicates that the current flowing through the battery, \(E\), is \(I_1\), identical to the current in \(R_1\). Similarly, KCL applied to nodes 1 and 2 gives \((I_1 I_2)\) as the current flowing through \(R_2\) and \((I_2 I_3)\) as the current conducted by \(R_4\). These currents are delineated in the circuit schematic diagram of Fig. (1.25).

2. The three circuit meshes are defined by the branch sequences, \(E_1 R_1 R_2\), \(R_2 R_3 R_4\), and \(R_4 R_5\). The corresponding mesh equations are
\[ E \ 5 \ \left( R_1 \ 1 \ R_2 \right) I_1 \ 2 \ R_2 I_2, \]
\[ 0 \ 5 \ 2 R_2 I_1 \ 1 \ \left( R_2 \ 1 \ R_3 \ 1 \ R_4 \right) I_2 \ 2 \ R_4 I_3, \]
\[ 0 \ 5 \ 2 R_4 I_2 \ 1 \ \left( R_4 \ 1 \ R_5 \right) I_3. \]

These three equations can be solved for \( I_1, I_2, \) and \( I_3, \) with the result that \( I_1 = 129.51 \) mA, \( I_2 = 22.46 \) mA, and \( I_3 = 5.18 \) mA. This solution expedites the calculation of all other branch currents, all branch voltages, and all node voltages. Specifically, the current conducted by \( R_2 \) is \((I_1, 2I_2) = 107.05 \) mA, and the current flowing in \( R_4 \) is \((I_2, 2I_3) = 17.28 \) mA. The voltage at node 1 is

\[ E_1 = R_2 \left( I_1 + 2I_2 \right) = 10.71 \text{ volts}, \]

and the voltage developed at node 2 is

\[ E_2 = R_4 \left( I_2 + 2I_3 \right) = 10.37 \text{ volts}. \]

The voltage at node 3 is, of course, the same as the power supply voltage, \( E; \) that is

\[ E_1 = E = 12 \text{ volts}. \]

(3). One of the three node voltages, \( E_1, E_2, \) and \( E_3, \) is known by virtue of the fact that the battery voltage, \( E, \) elevates node 3 above ground by a constant voltage whose value is 12 volts. Since the purpose of nodal analysis is the determination of the circuit node voltages, only two nodal equations need be written. With \( G_i \) designating the conductance, \( G_i = 1/R_i \) associated with the general resistance, \( R_i, \) KCL applied to nodes 1 and 2 gives

\[ G_1 E_1 = \left( G_1 \ 1 \ G_2 \ 1 \ G_3 \right) E_1 \ 2 \ G_3 E_2, \]

\[ 0 \ 5 \ 2 G_3 E_1 \ 1 \ \left( G_2 \ 1 \ G_3 \ 1 \ G_5 \right) E_2. \]

A simultaneous solution of these equations delivers results that are identical to the answers provided by mesh analysis.

(4). Tellegen's theorem offers another check on the propriety of the solutions documented in STEP #2. To this end, let \( p_{R_i} \) denote the power delivered to the resistance, \( R_i. \) Since \( p_{R_i} \) is the product of the voltage developed across, and the current flowing through, resistance \( R_i, \) with the understanding that such voltage and current are in the associated reference polarity convention,
The sum of these five delivered branch powers, \( P_{\text{dis}} = 1.554 \) watts, is the net power consumed by the five branch resistive network. This power must equate to the power, say \( P_E \), supplied by the battery of voltage \( E \). Indeed, \( P_E = P_{\text{dis}} \), since

\[
P_E = E \cdot I_1 = 1.554 \text{W}.
\]

The fact that \( P_E = P_{\text{dis}} \) does not prove that the branch current and node voltage solutions computed above are correct. But \( P_E = P_{\text{dis}} \) would have proven that these solutions are wrong.

**EXAMPLE (1.4)**

Adopt KCL as a means of solving for the node voltages of the circuit in Fig. (1.26). The parameters of the circuit are as follows, where the symbology, "KV" represents thousand of ohms or "kilo ohms":

- \( R_S = 300 \text{ V} \)
- \( R_I = 2.5 \text{ KV} \)
- \( R_E = 5 \text{ 10 V} \)
- \( R_C = 100 \text{ V} \)
- \( R_O = 5 \text{ 12 KV} \)
- \( R_L = 5 \text{ 5 KV} \)
- \( R_F = 6 \text{ KV} \)
- \( h_f = 5 \text{ 0.05} \)
- \( b = 5 \text{ 100} \)
- \( V_S = 5 \text{ 100 mV} \)

![Circuit Diagram](image)

**SOLUTION (1.4)**
The circuit in Fig. (1.26) has seven nodes, inclusive of the ground node to which the node voltages, \( E_1, E_2, E_3, E_4, E_5, \) and \( E_6 \) are referred. The circuit is more complicated than the structure examined in the preceding example owing to the presence of a voltage controlled voltage source \((h_r V_x)\) and a current controlled current source \((b I)\).

(1). The first step in the solution process is the determination of a minimum set of specific nodes to which KCL must be applied. To this end, note that \( E_1 \) is already known; that is, \( E_1 = 5 \text{ V}_S = 5 \text{ 100 mV} \). Since the purpose of nodal analysis is the evaluation of all circuit node voltages, the fact that \( E_1 \) is known a priori means that KCL need not be applied to node 1.

Note further that \( E_3 \) is not independent of \( E_4 \), since by KVL,

\[
E_3 = h_r V_x + E_4.
\]

Thus, KCL need be applied to node 3 or to node 4, but not to both nodes. While on the subject of relating \( E_3 \) -to- \( E_4 \), it is worthwhile remembering that the objective of KCL is to arrive at a set of independent relationships in terms of the node voltages of the circuit. The controlling voltage, \( V_x \), is not a node voltage. But it is related to the node voltages, \( E_5 \) and \( E_4 \), by the KVL expression,

\[
V_x = E_5 - E_4.
\]

It follows that \( E_3 \) can be related to circuit node voltages alone in accordance with

\[
E_3 = \left(1 - h_r\right) E_4 + h_r E_5.
\]

In similar fashion, the controlling variable, \( I \), of the current controlled current source, \( bI \), is expressible in terms of node voltages by observing that \( I \) flows from left -to- right through \( R_I \) and is therefore given by

\[
I = \frac{E_2 - E_3}{R_I} = 5 \frac{G_I}{E_2 - E_3} \left(E_2 - E_3\right),
\]

where conductance notation is adopted for the resistance, \( R_I \). Recalling the expression for the voltage, \( E_3 \), the controlled current, \( bI \), becomes

\[
b I = b G_I \left[E_2 - \left(1 - h_r\right) E_4 + h_r E_5\right].
\]
Since KCL need not be applied at node 1, and given that \( E_3 \) has been expressed in terms of \( E_4 \) and \( E_5 \), while \( bI \) has been cast in terms of \( E_2, E_4, \) and \( E_5 \), KCL need be applied only at nodes 2, 4, 5, and 6.

(2). For node 2,

\[
0 \ 5 \ G_S \left( E_2 \cdot V_S \right) \cdot 1 \ G_I \left( E_2 \cdot E_3 \right) \cdot 1 \ G_F \left( E_2 \cdot E_6 \right) .
\]

Observe that in addition to flowing through \( R_1 \), the current, \( G_I(E_2 E_3) \), flows through the VCVS, \( h_r V_x \), and flows into node 4. Thus, at node 4,

\[
G_I \left( E_2 \cdot E_3 \right) \cdot 5 \ G_E \cdot E_4 \cdot 2 \ bI \cdot I \cdot G_O \left( E_4 \cdot E_5 \right) .
\]

At nodes 5 and 6, KCL yields

\[
0 \ 5 \ bI \cdot I \cdot G_O \left( E_5 \cdot E_4 \right) \cdot 1 \ G_C \left( E_5 \cdot E_6 \right) ,
\]

\[
0 \ 5 \ G_L \cdot E_6 \cdot 1 \ G_C \left( E_6 \cdot E_5 \right) \cdot 1 \ G_F \left( E_6 \cdot E_2 \right) .
\]

(3). The variables, \( I \) and \( E_3 \), can be eliminated from the preceding four equations by using the relationships for \( bI \) and \( E_3 \) derived in STEP #2. The result is a system of four algebraic equations in the four unknown node voltages, \( E_2, E_4, E_5, \) and \( E_6 \). A simultaneous solution of the resultant system of equations produces

\[
E_2 = 5 \ 2301.07 \text{ mV} ,
\]

\[
E_4 = 5 \ 29.61 \text{ mV} ,
\]

\[
E_5 = 5 \ 28.40 \text{ V} ,
\]

\[
E_6 = 5 \ 28.10 \text{ V} .
\]

Since \( E_2, E_5, \) and \( E_6 \) are negative voltages, nodes 2, 5, and 6 lie below, not above, the ground reference potential of zero volts. It should also be noted that the magnitude of the voltages developed at nodes 5 and 6 is larger than the applied source voltage of 100 mV. This amplification of the input source voltage is due to the dependent sources, particularly the CCCS. The presence of this controlled source means that the circuit under consideration is actually an electrical model of a more complex network in which a current amplifier is apparently embedded. The network at hand is, in fact, active (capable of signal amplification), whereas networks divorced of controlled sources are passive and therefore incapable of boosting the amplitudes of input voltages or currents.
1.3.0. **CIRCUIT THEOREMS**

Of the numerous formal theorems that collectively comprise the circuit theory discipline, three are especially important to the study of linear electronic circuits and systems. These three theorems are the superposition theorem, Thévenin's theorem, and Norton's theorem.

1.3.1. **SUPERPOSITION**

Superposition theory applies to linear circuits and systems in which more than one source of independent energy is applied to produce measurable or computable responses. The sources of energy, which can be currents or voltages, are called the inputs to the circuit or system undergoing study. In electrical circuits, the responses are branch currents, branch voltages, or node voltages and are called the outputs. Superposition theory states that each response of a linear circuit or system can be determined as the sum of the responses generated by each independent energy source acting alone. This is to say that the observable response of a linear circuit or system excited by $N$ sources of energy is the superposition of the responses of each of the $N$ sources taken one at a time.

Superposition phenomena is commonplace in all practical electrical and electronic circuits. Consider, for example, a compact disc (CD) played on a CD player that is connected to a stereo system. If the recorded music consists of a vocalist, a guitarist, and a pianist, it is natural to expect to hear vocal singing, guitar music, and the sounds of a piano at the speaker, or output, of the stereo system. If any one of the three sources of musical sound does not emanate from the speaker, the stereo system is considered inferior in the sense of its apparent inability to reproduce recorded information faithfully. In effect, superposition with respect to the various input sources of recorded information is expected –indeed demanded– of a quality stereo system.

Unfortunately, superposition phenomena can often impact electronic systems deleteriously. In the stereo system hypothesized above, improperly shielded and inordinately long interconnects between the CD player and the stereo preamplifier are vulnerable to electromagnetically coupled spurious signals. Thus, audio frequency signals from proximate fluorescent lights or nearby appliances can couple parasitically to the preamplifier. The result is a net speaker response reflecting a superposition of the desired recorded music and the undesired signal spurs.

Superposition underlies the complete solution to the $n$th order, linear, ordinary differential equation that interrelates the time domain response and inputs of an $n$th order linear circuit having distinguishable nodes and branches. Mathematics courses teach that the complete time domain solution of this form of an I/O relationship is the sum of the homogeneous and particular solutions. In the jargon of electrical engineering, the homogeneous solution is more commonly known as the zero input response or natural response, and the particular solution is called the zero state response or the forced response. The zero input response, say $y_{zi}(t)$, is found by setting all sources of independent energy applied to the circuit undergoing study, and thus the net effective forcing function, $f(t)$, of the differential equation, to
zero. On the other hand, the zero state response, \( y_{zs}(t) \), accounts for only the specific time domain nature of the inputs to the circuit or system undergoing study. Thus, the complete time domain solution, say \( y(t) \), to the differential I/O equation of an \( n \)th order linear circuit is

\[
y(t) = y_{zi}(t) + y_{zs}(t) .
\]  

(1-39)

The scenario just described is more than a mere set of rules for solving a differential equation; it is, in fact, a consequence of superposition theory. To understand this contention, recall that of the nine basic elements that can be embedded in a linear circuit, only the capacitor and the inductor have volt ampere characteristics in which derivatives of branch variables appear. Thus, the I/O relationship of a linear circuit is a differential equation only because some of the branch elements of the circuit are capacitors or inductors. But capacitors and inductors are energy storage elements. This fact implies that the net response, at any general time \( t \), of a linear circuit containing energy storage elements is attributed to two phenomena. The first of these phenomena is the obvious one; namely, the actual input or inputs applied to the circuit drive the circuit response to a certain value. The second derives from the fact that at time \( t \), each capacitor remembers its voltage immediately prior to time \( t \) and similarly, each inductor remembers its initialized current. The electrical ramifications of these initialized states are energy sources that are manifested in a voltage in the case of a capacitor and a current in the case of an inductor. Like the actual input or inputs to a linear circuit, these capacitor voltages and inductor currents contribute to the net circuit response at time \( t \). The zero input response, which determines circuit output in the presence of zero applied inputs, is a measure of the impact exerted on circuit response by initial capacitor voltages and initial inductor currents. In contrast, the zero state response quantifies the net output response due to the actual inputs applied to the circuit. The individual evaluation of these two forms of circuit responses, followed by their summation, as per (1-39), to ascertain the net circuit response, is a direct exploitation of superposition theory.

**EXAMPLE (1.5)**

Three signal sources, \( V_{ST} \), \( V_{SN} \), and \( I_{SN} \), are applied to the circuit shown in Fig. (1.27a). Use superposition theory to determine the net output voltage response, \( V_{01} \). [The output voltage, \( V_{02} \), is used in an assigned problem at the conclusion of this chapter.]

**SOLUTION (1.5)**

The circuit in Fig. (1.27a) can be analyzed straightforwardly through a direct application of KCL and KVL. The results obtained are identical to those that derive by superimposing the individual effects of \( V_{ST} \), \( V_{SN} \), and \( I_{SN} \).

(1). Fig. (1.27b) is the equivalent circuit pertinent to computing the constituent output, \( V_{vst} \), generated solely by the signal source, \( V_{ST} \). Note that the voltage source, \( V_{SN} \), is removed by replacing \( V_{SN} \) with a short circuit, while the current source, \( I_{SN} \), is removed by supplanting it with an open circuit. By KCL, the current flowing through the resistance,
\( R_E \) is \((b11)I\). Then, KVL gives

\[ I = \frac{V_{ST}}{R_S + R_L + (b11)R_E}. \]

Since KVL also produces

\[ V_{vst} = 2b R_L I, \]

it follows that

\[ V_{vst} = 2 \frac{b R_L V_{ST}}{R_S + R_L + (b11)R_E} \]

is the contribution to the net response spawned exclusively by \( V_{ST} \).
Fig. (1.27).  (a). Circuit Studied In EXAMPLE (1.5) To Demonstrate The Utility Of Superposition.  (b). Equivalent Circuit For Computing The Output Due Only To The Voltage, $V_{ST}$.  (c). Equivalent Circuit For Computing The Output Due Only To The Voltage, $V_{SN}$.  (d). Equivalent Circuit For Computing The Output Due Only To The Current, $I_{SN}$.

(2). Fig. (1.27c) is the equivalent circuit for computing the output, $V_{vsn}$, due solely to the signal source, $V_{SN}$. Note that the voltage source, $V_{ST}$, and the current source, $I_{SN}$, are set to zero. The voltage, $V_{vsn}$, is easily shown to be
\[
V_{\text{vsn}} = \frac{1}{b R_L} \frac{b R_L V_{\text{SN}}}{R_S 1 R 1 (b l 1) R_E}.
\]

(3). Fig. (1.27d) is the equivalent circuit for computing the output, \(V_{\text{isn}}\), attributed to the independent current source, \(I_{\text{SN}}\). Both of the voltage sources, \(V_{\text{ST}}\) and \(V_{\text{SN}}\), are now set to zero. The resultant voltage, \(V_{\text{isn}}\), is

\[
V_{\text{isn}} = \frac{1}{R_L} I_{\text{SN}}.
\]

(4). By superposition theory, the net response is

\[
V_{\text{01}} = V_{\text{vst}} V_{\text{vsn}} V_{\text{isn}}.
\]

Letting

\[
G_{\text{me}} = \frac{D}{b R_S R L 1 (b l 1) R_E},
\]

the substitution of the results for \(V_{\text{vst}}\), \(V_{\text{vsn}}\), and \(V_{\text{isn}}\) into the equation for \(V_{\text{01}}\) produces

\[
V_{\text{01}} = 2 G_{\text{me}} R_L \left( V_{\text{ST}} 2 V_{\text{SN}} 2 \frac{I_{\text{SN}}}{G_{\text{me}}} \right).
\]

One advantage of using superposition theory to arrive at the response of a circuit excited by several sources of independent energy is that it inherently isolates the individual effects of the applied sources. In the preceding example, superposition underscores the fact that the voltage sources, \(V_{\text{ST}}\) and \(V_{\text{SN}}\), have an equal magnitude, but opposite algebraic sign, effect on the net response, \(V_{\text{01}}\). Moreover, for a large effective transconductance, \(G_{\text{me}}\), the impact on \(V_{\text{01}}\) of the current source, \(I_{\text{SN}}\), is negligible in comparison to the magnitude of the effects exerted by \(V_{\text{ST}}\) and \(V_{\text{SN}}\).

1.3.2. THÉVENIN AND NORTON THEOREMS

Circuit analyses frequently entail calculations of either voltages developed across, or currents flowing through, a branch element for various values of the branch element or even for different types of branch elements. Obviously these calculations can be performed by analyzing the circuit in which the subject branch is embedded for each and every branch element of interest. Such a computational tack can be tedious and inefficient. It is tedious if the complete analysis of the circuit at hand requires the simultaneous solution of more than three equations, and it is inefficient if circuit branch variables other than those associated with the subject variable element are of no interest. For the case in which the variable branch element is driven by a linear circuit, Thévenin's theorem and its companion, Norton's theorem,
provide a useful and insightful alternative to the computational tedium entailed by repetitive circuit analyses.
1.3.2.1. **Thévenin's Theorem**

Thévenin's theorem states that two terminals of any linear circuit can be modeled by a voltage source in series with a resistance. The voltage source appearing in the Thévenin equivalent circuit with respect to the two terminals of interest is called the Thévenin voltage, \( V_{th} \), and the resistance, say \( R_{th} \), is termed the Thévenin resistance. If the two terminals of interest are extracted from a memoryless circuit, \( V_{th} \) and \( R_{th} \) are constants. On the other hand, a circuit containing capacitors and/or inductors produces \( V_{th} \) and \( R_{th} \) that are functions of the frequencies of the voltage and current signals applied to the circuit. In this case, \( V_{th} \) and \( R_{th} \) are cast as functions of transformed frequency variables and are respectively referred to as the transform of the Thévenin voltage and the Thévenin impedance.

![Diagram of Energized Linear Circuit with Thévenin Equivalent Circuit](image)

**Fig. (1.28).** (a). Diagram Showing A Particular Branch Of An Energized Linear Circuit. (b). Schematic Diagram Of The Thévenin Equivalent Circuit With Respect To Terminals "A" And "B" In The
The essence of Thévenin's theorem is illustrated by Fig. (1.28). In Fig. (1.28a), a linear circuit energized by voltage and/or current sources drives a presumably variable branch that is designated as a general load. The load, which need not have linear volt ampere characteristics, is connected between nodes "A" and "B" of the circuit. The circuit establishes a voltage, \( V_L \), across the load and sustains a current, \( I_L \), flowing through the load, as indicated. Regardless of the number of branches and nodes that collectively define the topology of the energized linear circuit, Thévenin's theorem allows for its replacement by the simple two branch equivalent circuit of Fig. (1.28b). The two branch Thévenin equivalent circuit is not likely to be topologically identical to the original structure. It is therefore important to understand that the configuration in Fig. (1.28b) is, in general, "equivalent" to that of Fig. (1.28a) only insofar as terminals "A" and "B" are concerned. Specifically, both networks in Fig. (1.28) produce the same load voltage, \( V_L \), from terminal "A"-to- terminal "B," and the same load current, \( I_L \), flowing from terminal "A"-to- terminal "B."

The scenario for determining \( V_{\text{th}} \) and \( R_{\text{th}} \) for the energized linear circuit is a direct exploitation of the Thévenin concept. In particular, the model drawn in Fig. (1.28b) is valid for any and all loads connected to terminals "A" and "B." Consider the case in which the load is a test current source, say \( I_x \), as depicted in Fig. (1.29a). In a circuit theoretic sense, this current, which results in a voltage, say \( V_x \), across the subject terminals, can have any arbitrary value. But if the test source is utilized in the laboratory to measure \( V_{\text{th}} \) and \( R_{\text{th}} \), \( I_x \) must be sufficiently small to ensure that the linearity properties of the energized circuit are not compromised.

Recalling Fig. (1.28b), the equivalent circuit with respect to terminals "A" and "B" of the structure in Fig. (1.29a) is as offered in Fig. (1.29b). KVL yields

\[ V_x = V_{\text{th}} + R_{\text{th}} I_x \]  \hspace{1cm} (1-40)

which suggests that \( V_x \) \( \neq \) \( V_{\text{th}} \) when \( I_x \neq 0 \). But \( I_x \neq 0 \) reflects an open circuited load termination. In turn, the corresponding voltage developed from terminal "A"-to- terminal "B," under the case of an open circuit (or no load) across this terminal pair is the desired Thévenin voltage from terminal "A"-to- terminal "B" of the energized linear circuit, as illustrated in Fig. (1.29c).

Equation (1-40) also underscores the fact that \( R_{\text{th}} \) is the ratio of \( V_x \)-to- \( I_x \), when \( V_{\text{th}} \neq 0 \). Now, \( V_{\text{th}} \) is the open circuit terminal voltage identified in Fig. (1.29c). Since this terminal voltage is produced exclusively by an energized linear circuit, \( V_{\text{th}} \) is the superposition of the effects of all independent voltage and current sources applied to the circuit undergoing examination. Thus, if these sources of independent energy are all set to zero, \( V_{\text{th}} \) necessarily reduces to zero. The result is the Thévenin equivalent circuit of Fig. (1.29d), for which Ohm's law delivers

\[ R_{\text{th}} = \frac{V_x}{I_x} \]  \hspace{1cm} (1-41)
Fig. (1.29). (a). Application Of A Test Current, $I_x$, From Terminal "B"-To- Terminal "A" Of An Energized Linear Circuit. (b). Thévenin Equivalent Circuit, With Respect To Terminals "A" And "B," Of The Network In (a). (c). The Circuit Of (a), But With $I_x$ Set To Zero. The Resultant Open Circuit Voltage From Terminal "A"-To- Terminal "B" Is The Thévenin Voltage, $V_{th}$. (d). Thévenin Equivalent Circuit, With Respect To Terminals "A" And "B," Of The Network In (a), But With All Sources Of Independent Energy Set To Zero.

**EXAMPLE (1.6)**

Find the Thévenin equivalent circuit that drives the resistance, $R_O$, in the circuit given in Fig. (1.30). Use this model to determine the voltage, $V_O$, for $R_O 5 100$ V, 10 kV, and 100 kV. The other branch elements in the circuit are:

\[
\begin{align*}
R & 5 1.5 \text{ kV} \\
R_L & 5 5 \text{ kV} \\
R_F & 5 5 \text{ V} \\
V_S & 5 10 \text{ mV}
\end{align*}
\]

**SOLUTION (1.6)**

The Thévenin equivalent circuit contains two branch elements. One of these is a generator representing the Thévenin voltage, $V_{th}$, at the terminals of interest, and the other is Thévenin resistance, $R_{th}$, facing the load that is connected across the subject terminals.

(1). Fig. (1.30b) is the circuit pertinent to the computation of $V_{th}$. Note that the load, which is the resistance, $R_O$, in this case, has been supplanted
by an open circuit. KVL verifies

Fig. (1.30). (a). Circuit Addressed In EXAMPLE (1.6). (b). Circuit Used To Compute The Thévenin Voltage "Seen" By $R_O$. (c). Circuit Used To Compute The Thévenin Resistance "Seen" By $R_O$. (d). Thévenin Equivalent Circuit Driving The Resistance, $R_O$. 
\[ V_S = 5 \left[ R \left( b11 \right) R_E \right] I, \]
\[ V_{th} = 2 b R_L I 2 \left( b11 \right) R_E I, \]

whence,
\[ V_{th} = 2 \left[ \frac{b R_L \left( b11 \right) R_E}{R \left( b11 \right) R_E} \right] V_S. \]

The numerical answer yielded by this expression is \( V_{th} = 22.50 \) volts.

2. Two procedural steps precede the computation of the Thévenin resistance, \( R_{th} \). First, all independent sources in the circuit of Fig. (1.30a) are clamped to zero. In the present example, only one such source, \( V_S \), is present. Second, the subject load, which here is the resistance, \( R_O \), is replaced by a test current source, \( I_x \). The immediate effect of this current source is to establish a voltage, \( V_x \), in disassociated reference polarity with \( I_x \), across its terminals. The resultant equivalent circuit used to calculate \( R_{th} \) is the structure provided in Fig. (1.30c). An analysis of this circuit gives
\[ 0 = 5 \left[ R \left( b11 \right) R_E \right] I 2 R_E I_x, \]
\[ V_x = 5 R_L \left( I \left( b11 \right) \right) \left[ R_E \left( b11 \right) I \right]. \]

A solution of the first of these two equations for the current, \( I \), followed by the substitution of this result into the second equation, leads to a relationship for which the ratio, \( V_x/I_x \), which is the desired Thévenin resistance, can be cast exclusively in terms of the branch element parameters of the original network. Following algebraic manipulation, the result is
\[ R_{th} = \left[ \frac{V_x}{I_x} \right] \left[ \frac{R \left( b11 \right) R_E}{R \left( b11 \right) R_E} \right]^2 \left( b11 \right), \]
where "|" denotes in parallel with. Numerically, \( R_{th} = 3.757 \) ohms.

3. Fig. (1.30d) is the Thévenin equivalent circuit that drives the resistance, \( R_O \). This simple model gives
\[ V_O = 5 \left( \frac{R_O}{R_O \left( 1 R_{th} \right)} \right) V_{th}. \]

For \( R_O = 100 \) V, \( V_O = 264.7 \) mV, while \( R_O = 10 \) K delivers \( V_O = 21.82 \) V. Finally, \( R_O = 100 \) K delivers \( V_O = 22.41 \) V.
Observe that the final results follow forthwith from the voltage divider expression that relates the desired voltage to the Thévenin voltage and Thévenin resistance in the pertinent Thévenin equivalent circuit. The tradeoff for this trivial computation is the need to analyze two circuits: one appropriate to the computation of \( V_{th} \) and the other appropriate to the calculation of \( R_{th} \). Generally, but not always, this tradeoff is more easily expedited than is a repetitive analysis of the entire circuit to which the variable load is connected.

1.3.2.2. **Norton's Theorem**

When the Thévenin resistance associated with a terminal pair of an energized linear circuit is very large, it may prove difficult or even impossible to compute or measure the Thévenin voltage. In these cases, Norton's theorem offers a pragmatic alternative to Thévenin's theorem. Norton's theorem states that two terminals of any linear circuit are electrically equivalent to a current source in shunt with a resistance. The current source appearing in the Norton equivalent circuit with respect to the two terminals of interest is called the Norton current, \( I_{no} \). The shunting resistance is identical to the Thévenin resistance.

Fig. (1.31b) overviews the Norton equivalent circuit at terminals "A" and "B" of the generalized circuit abstracted in Fig. (1.28a), which is repeated in Fig. (1.31a) for convenience. Insofar as load variables \( V_L \) and \( I_L \) are concerned, the model of Fig. (1.31a) is equivalent to the circuit of Fig. (1.31a). Moreover, since the Thévenin circuit of Fig. (1.29b) is also equivalent to Fig. (1.31a), with respect to predicting the load voltage and current, the Norton and Thévenin equivalent circuits must be identical with respect to a mathematical emulation of the observable electrical characteristics at terminals "A" and "B."

The foregoing observation implies a relationship between the Norton equivalent current, \( I_{no} \), and the Thévenin equivalent voltage, \( V_{th} \). It also allows for a physical interpretation of the Norton current. To investigate these contentions, consider the network of Fig. (1.31a) for the case of a short circuit load imposed between terminals "A" and "B." The current conducted by the short circuit is designated \( I_{sc} \). This situation is shown in Fig. (1.32a), while Figs. (1.32b) and (1.32c) give the relevant Thévenin and Norton equivalent circuits, respectively. Since the short circuit constrains the voltage between terminals "A" and "B" to zero, Fig. (1.32b) verifies that

\[
I_{sc} = \frac{V_{th}}{R_{th}}.
\]

(1-42)

In Fig. (1.32c), no current can flow through the shunting Thévenin resistance and thus,

\[
I_{sc} = I_{no};
\]

(1-43)

that is, the Norton equivalent current is the current that flows in a short circuited load interconnected between terminals "A" and "B" of the energized network of Fig. (1.31a).
Equations (1-42) and (1-43) combine to deliver

\[
V_{th} = R_{th} I_{no},
\]  

(1-44)

which is the previously conjectured relationship between the Thévenin voltage and the Norton current.
Fig. (1.32). (a) Diagram Showing A Short Circuited Branch Of An Energized Linear Circuit. (b) Thévenin Equivalent Circuit With Respect To Terminals “A” and “B” Of The Circuit In (a). (c) Norton Equivalent Circuit With Respect To Terminals “A” and “B” Of The Circuit In (a).

**EXAMPLE (1.7)**

Find the Norton equivalent circuit that drives the resistance, $R_O$, in the circuit given in Fig. (1.30a). Use the results of Example (1.6) to confirm that the Norton equivalent current in this model satisfies (1.44).

**SOLUTION (1.7)**

The Thévenin resistance, $R_{th}$ seen by the circuit resistance, $R_O$, in Fig. (1.30)
has been computed as per STEP #2 of EXAMPLE (1.6). Thus, only the short circuit, or Norton, current need be calculated to satisfy the requirements of this problem.

\begin{align*}
\text{has been computed as per STEP #2 of EXAMPLE (1.6). Thus, only the short} \\
\text{circuit, or Norton, current need be calculated to satisfy the requirements of} \\
\text{this problem.}
\end{align*}

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig1.33}
\caption{(a). Circuit Of Fig. (1.30a), With The Resistance, \( R_O \), Replaced By A Short Circuit To Allow For The Calculation Of The Norton Current, \( I_{no} \). (b). Norton Equivalent Circuit "Seen" By The Resistance, \( R_O \), In The Circuit Of Fig. (1.30a).}
\end{figure}

\textbf{(1).} Fig. (1.33a) is the circuit of Fig. (1.30a) redrawn to delineate the branch in which the Norton current, \( I_{no} \), flows. This branch is a short circuit that replaces the resistance, \( R_O \), in the original circuit diagram. By KVL,

\begin{align*}
0 & \Rightarrow R_L (b I I_{no}) + R_E [(b I I_{no})] = V_S, \\
V_S & \Rightarrow R_L (b I I_{no}) + R_E [(b I I_{no})] = V_S.
\end{align*}

If the solution for the current, \( I \), in the first of these two equations is substituted into the second expression, an equation relating \( V_S \) exclusively to the Norton current, \( I_{no} \), results. The solution of this
resultant equation for $I_{no}$ gives

$$I_{no} = 2 \left( \frac{b R_L + 1}{R_L + R_E} \right) \left( \frac{b R_L + 1}{R_L + R_E} \right) V_S.$$ 

Numerically, $I_{no} = 2664.5$ microamperes ($mA$).

To check the propriety of this calculation, recall from EXAMPLE (1.6) that the Thévenin voltage, $V_{th}$, and Thévenin resistance, $R_{th}$, "seen" by $R_O$ are $22.50$ volts and $3,757$ ohms, respectively. Using (1-44), $I_{no} = \frac{V_{th}}{R_{th}} = \frac{22.50}{3757} \approx 2664.5$ mA, as expected.

(2). The Norton equivalent circuit facing the subject branch resistance, $R_O$, is given in Fig. (1.33b). Since $R_{th}$ and $R_O$ are in shunt with one another in this model,

$$V_O = I_{no} \left( \frac{R_{th} + R_O}{R_{th} + R_O} \right).$$

Observe that (1-44) reduces this expression to

$$V_O = \left( \frac{R_O}{R_O + 1} \frac{1}{R_{th}} \right) V_{th},$$

which is identical to the voltage expression obtained in STEP #3 of the preceding example. It follows that the numerical answers for $V_O$, corresponding to the three considered values of $R_O$, remain the same as previously computed.

1.3.2.3. APPLICATIONS

Aside from simplifying the analysis of cumbersome circuits, the Thévenin and Norton theorems conduce insights into the electrical behavior of practical two terminal energy sources and entire electrical systems. For example, consider a simple battery driving a load resistance of $R_L$, as shown in Fig. (1.34a). It is intuitively evident that a short circuited load, as reflected by the condition, $R_L = 0$, reduces the load voltage, $V_L$, to zero. But if the battery were to be modeled by an ideal constant voltage source, as offered in Fig. (1.34b), this intuitive conclusion cannot be reached. In fact, Fig. (1.34b) proffers a conflict. On the one hand, the short circuited load implies $V_L = 0$, while on the other hand, KVL yields $V_L = E$, where $E$ is presumably non zero. The problem is that Fig. (1.34b) is an incorrect equivalent circuit of the network in Fig. (1.34a), for Thévenin's theorem requires that any two terminals of a linear circuit be replaced by a voltage source in series with a resistance. Accordingly, the model in Fig. (1.34c) is the appropriate electrical representation, where the Thévenin resistance, $R$, is
viewed as the internal resistance of the two terminal battery of Fig. (1.34a), and \( E \) is the open circuit voltage of the battery. In other words, \( E \) is the voltage developed across the load resistance terminals if and only if the load is replaced by an open circuit. This assertion and the fact that \( V_L = 0 \) for \( R_L = 0 \) are confirmed by KVL and Ohm's law, which, when applied to the circuit of Fig. (1.34c), gives the voltage divider expression,

\[
V_L = E \left( \frac{R_L}{R_L + R} \right).
\]  

(1-45)

The modeling contentions made in regard to sources of constant voltage apply equally well to time varying voltages.

Just as a source of constant voltage cannot be modeled by a constant voltage source alone, a constant current source cannot be represented by only a constant current generator. Consider the case of a load resistance, \( R_L \), connected to a current source, as depicted in Fig. (1.35a). If this system is modeled by the equivalent circuit postulated by Fig. (1.35b), an inconsistency results when the load is open circuited. In particular, if \( R_L \to \infty \), the current, \( I_L \), flowing through the load is, by definition, zero. But KCL applied to the circuit of Fig. (1.35b) gives \( I_L = 0 \). The problem is that Norton's theorem requires that the current source in Fig. (1.35a) be represented by an ideal constant current source, \( I \), in shunt with a resistance, \( R \), as given in Fig. (1.35c). In this case, \( I \) is viewed as the short circuit current delivered by the current source, and \( R \) is the internal resistance of the current source. These interpretations are supported by KVL, which yields, for the circuit in Fig. (1.35c), the current divider relationship,

\[
I_L = I \left( \frac{R}{R + R_L} \right).
\]  

(1-46)

The analytical explanation of why amplifiers fail to deliver identical gains for different load and source terminations is yet another practical application of Thévenin's and
Norton's theorems. An investigation of this contention requires an understanding of how Thévenin's or Norton's theorems can be exploited to deduce a practical model of a linear amplifier. To this end, consider the active system of Fig. (1.36a), which depicts a linear amplifier terminated at its output in a load resistance, $R_L$, and driven at its input by a signal whose Thévenin representation is a voltage source, $V_{ST}$, placed in series with a
resistance, $R_S$. The signal voltage, $V_{ST}$, gives rise to the output voltage, $V_O$, developed across the load resistance, $R_L$. It also establishes the voltage, $V_I$, across the amplifier input port, which is the terminal pair, $1/1'$.

By Thévenin's theorem, the two output port terminals, $2/2'$, of the amplifier are electrically equivalent to a voltage source, say $V_{tho}$, in series with a resistance, $R_{out}$, as delineated in Fig. (1.36b). The Thévenin resistance, $R_{out}$, is termed the output resistance of the amplifier. It is evaluated in concert with the discussions surrounding Fig. (1.29), with all independent sources of energy (only one such source, $V_{ST}$, appears in this case) set to zero. The output port Thévenin voltage, $V_{tho}$, is the open circuit ($R_L \rightarrow \infty$) output voltage generated by $V_{ST}$. Since the amplifier is a linear circuit, $V_{tho}$ is proportional to $V_{ST}$. But the amplifier input port voltage, $V_I$, is also linearly dependent on $V_{ST}$. Thus, the Thévenin output voltage source can be viewed as a voltage controlled voltage source (VCVS) whose value is $V_{tho} \equiv a_{vo} V_I$. The proportionality constant, $a_{vo}$, is a function of the parameters indigenous to the linear amplifier alone. It is therefore independent of the load and source terminations, $R_L$ and $R_S$, respectively, and it is meaningfully termed the open circuit voltage gain of the amplifier. Specifically, $a_{vo}$ is the ratio of the open circuit voltage developed across the output port of the amplifier -to- the voltage appearing across the input port of the linear amplifier.

The two terminals, $1/1'$, that comprise the input port of the amplifier can likewise be replaced by a Thévenin equivalent circuit. In this case, however, the Thévenin input voltage facing the source subcircuit is zero owing to the lack of independent energy sources both within the amplifier and at the output port. Accordingly the Thévenin input circuit consists merely of a resistance, $R_{in}$, as shown in Fig. (1.36c). This resistance, termed the input resistance of the amplifier, emulates the net effective resistance seen by the signal source subcircuit between terminals $1/1'$. It is evaluated with the output port terminated in the resistance, $R_L$. The input port Thévenin equivalent circuit of Fig. (1.36c) may now be coalesced
with the amplifier output port equivalent circuit of Fig. (1.36b) to form the amplifier model offered in Fig. (1.36d).

\[ V_{St} \]
\[ R_s \]
\[ V_i \]
\[ V_{th} \]
\[ 5a_{vo}V_i \]
\[ R_{out} \]
\[ V_o \]
\[ R_l \]

(a). Linear Amplification System Operating Between A Source Resistance, \( R_s \), And A Load Resistance, \( R_l \). (b). Thévenin Equivalent Circuit For The Output Port Of The Amplifier. (c). Thévenin Equivalent Circuit For The Input Port Of The Amplifier. (d). Equivalent Circuit For The Entire Active System Of (a).

KVL applied to the model of Fig. (1.36d) gives the two voltage divider expressions,
These two expressions combine to deliver an overall amplifier voltage gain, \( A_V = \frac{V_O}{V_{ST}} \), of the form,

\[
A_V = \frac{V_O}{V_{ST}} \left( \frac{R_{in}}{R_{in} \frac{1}{R_S}} \right) \left( \frac{R_L}{R_L \frac{1}{R_{out}}} \right) a_{vo} V_I.
\] (1-47)

Equation (1-48) shows that the open circuit voltage gain, \( a_{vo} \), of the amplifier is attenuated by the product of two voltage dividers: one attributed to the input circuit where the signal source of internal resistance, \( R_S \), is applied, and one due to the output circuit where the load resistance, \( R_L \), is incident. In particular, a source resistance that is large in comparison with the amplifier input resistance, \( R_{in} \), and/or a load resistance that is small in comparison with the amplifier output resistance, \( R_{out} \), results in an effective system voltage gain that is substantively smaller than the available gain, \( a_{vo} \), of the amplifier.

**EXAMPLE (1.8)**

The linear amplifier in the system configuration of Fig. (1.37a) has an input resistance of \( R_i \), an output resistance of \( R_o \), and an open circuit voltage gain of \( 2k_o \), where \( k_o \neq 0 \). Derive a general expression for the system voltage gain, \( A_V = \frac{V_O}{V_{S}} \). Simplify this result for the special case of an amplifier with a very large open circuit voltage gain; that is, \( k_o \rightarrow \infty \).

**SOLUTION (1.8)**

Using the model of Fig. (1.36d), the equivalent circuit of the system in Fig. (1.37a) is as depicted in Fig. (1.37b). Note that an account of the negative nature of the open circuit voltage gain has been made by reversing the polarity of the VCVS in the amplifier model.

(1). KVL applied to the output mesh of the equivalent circuit in Fig. (1.37b) reveals

\[
V_O = 2k_o V_I 2 R_o \left( \frac{V_O}{R_L} \right) 1 R_F \left( \frac{V_I \cdot 2}{R_L} \right),
\]

whence,

\[
\frac{V_I}{R_{in}} = 5 \left( \frac{R_F 1 R_L 1 R_o}{R_F 2 \ k_o R_{in}} \right) \left( \frac{V_o}{R_L} \right).
\]
For the input mesh,

\[
\begin{align*}
\text{V}_S & = 5 \left( \frac{R_S}{R_i} \right) \left( \frac{V_i}{R_i} \right) \left( \frac{R_i}{R_{in}} \right) \left( \frac{V_o}{R_L} \right) \frac{V_i}{R_i}.
\end{align*}
\]

The combination of the preceding two relationships leads to the desired voltage gain result, which is expressible as:

\[
A_V = 5 \frac{V_o}{V_S} \frac{2 k_o}{R_i} \left( \frac{R_i}{R_{in}} \right) \left( \frac{R_L}{R_i} \right) \left( \frac{R_o}{R_L} \right) \left( \frac{11 H_{fe}}{11 H_f} \right),
\]

Fig. (1.37). (a) Active System Addressed In EXAMPLE (1.8). (b) Equivalent Circuit Of The System In (a).
where

\[ H_{f0} = 2 \frac{R_F}{k_o R_i}, \]

and

\[ H_f = \frac{1}{11} \left( \frac{R_F}{R_S 1 R_i} \right) \left( \frac{R_S}{R_L 1 R_o} \right) \left( \frac{11 k_o R_i}{R_S} \right). \]

(2) If \( k_o \to \infty \), \( H_{f0} \to 0 \), and

\[ H_f \to k_o \left( \frac{R_F}{R_S 1 R_i} \right) \left( \frac{R_i}{R_L 1 R_o} \right). \]

It follows that in the limit of a very large magnitude of amplifier open loop gain,

\[ \lim_{k_o \to \infty} A_v = 2 \frac{R_i}{R_F}, \]

which is invariant with the amplifier input and output resistances, the amplifier open loop gain, and the internal resistance of the signal source.

It should be noted that \( R_F = 0 \) renders \( H_{f0} = H_f = 0 \). Under this condition, the voltage gain result found in STEP #2 reduces to an expression whose form is identical to the generalized voltage gain relationship in (1-48). This reduction reflects engineering expectation, since \( R_F = 0 \) collapses the system of Fig. (1.37a) to a common ground, phase inverted (because \( a_{v0} = k_o = 0 \)) version of the original system depicted in Fig. (1.36a).

1.4.0. **ANALYSIS OF CIRCUITS WITH MEMORY**

There are two components to the branch current, branch voltage, or node voltage response of any linear circuit containing energy storage elements. One of these components is the zero state response, \( y_{zs}(t) \), which is the linear superposition of the individual electrical effects of each independent voltage or current that is applied to the circuit. For the case of a single source of independent energy, say \( x_s(t) \), as abstracted in Fig. (1.38), \( y_{zs}(t) \) is a linear function of \( x_s(t) \). Specifically, its time domain form is precisely the same as the time dependence of \( x_s(t) \). Thus, if \( x_s(t) \) is a constant, \( y_{zs}(t) \) is also a constant, the value of which is proportional to the amplitude of \( x_s(t) \). Similarly, if \( x_s(t) \) is a ramp function, \( y_{zs}(t) \) is likewise a ramp, if \( x_s(t) \) is a
sinusoid, \( y_{zs}(t) \) is a sinusoid (most likely a sinusoid whose amplitude and phase angle differ from those of the input sinusoid), and so forth.

![Fig. (1.38). Symbolic Depiction Of The Time Domain Nature Of The Response Of A Linear Circuit Excited By A Single Source Of Input Excitation.](image)

The second component of the response of a linear circuit containing memory is the zero input response, \( y_{zi}(t) \). The zero input response is attributed solely to the electrical ramifications of initial energy stored as charges on circuit capacitors and magnetic flux associated with circuit inductors. Thus, if the independent signal source, \( x_s(t) \), is applied at time \( t = 0 \), \( y_{zi}(t) \) represents the electrical effects of the time \( t = 0 \) values of initial voltages appearing across circuit capacitors and initial currents flowing through circuit inductors. It is important to understand that since \( y_{zi}(t) \) is generated as a result of voltages developed across capacitors and currents flowing through inductors immediately prior to the application of the independent source of input energy, \( x_s(t) \), \( y_{zi}(t) \) is not a linear function of \( x_s(t) \). This means that despite the linear nature of the network abstracted in Fig. (1.38), the amplitude of the net response,

\[
y(t) = y_{zi}(t) + y_{zs}(t),
\]

is not proportional to the amplitude of \( x_s(t) \). Instead, only the zero state response, \( y_{zs}(t) \), is linearly dependent on the independent signal source, \( x_s(t) \).

In the circuit of Fig. (1.38), let \( n \) be the number of capacitor voltages and inductor currents that can be independently stipulated at time \( t = 0 \). For this so called nth order linear circuit, the zero input response, \( y_{zi}(t) \), is of the form,

\[
y_{zi}(t) = \sum_{i=1}^{n} k_i e^{s_i t},
\]

which gives a net circuit response, \( y(t) \), of

\[
y(t) = \sum_{i=1}^{n} k_i e^{s_i t} y_{zs}(t).
\]
In (1-50) and (1-51) the $k_i$ are related to the initial capacitor voltages and initial inductor currents, as well as to the branch element parameters, of the circuit. Moreover, each of the $(2s_i)$ is termed a pole, or a critical frequency, of the circuit. These $(2s_i)$ can be real, complex, or imaginary numbers. But physical realizability of the circuit dictates that for each non-real $(2s_i)$, there must be a companion pole, say $(2s_{i1})$, that is the complex conjugate of $(2s_i)$\[7\].

Analog circuits are designed to process given input signals in a prescribed fashion; that is, they are designed to produce a specified zero state output in response to a given input signal. In the context of (1-51) and Fig. (1.38), this design criterion implies the desirability of an ultimately vanishing, and perhaps even quickly vanishing, zero input response. From (1-51), an ultimately nulled zero input response is assured if

$$Re(2s_i) < 0; \quad (1-52)$$

that is, all real poles must be negative numbers and all complex poles must have negative real parts. A circuit subscribing to (1-52) is said to be asymptotically stable. After a sufficiently long time period, the electrical effects of initial conditions imposed on energy storage elements disappear in a properly designed, asymptotically stable circuit. Such a circuit therefore produces a net output response that ultimately reflects the input excitation in accordance with prescribed signal processing criteria.

A circuit is unstable if it possesses at least one pole such that

$$Re(2s_i) \geq 0. \quad (1-53)$$

In this case, the corresponding terms in the first function on the right hand side of (1-51) are boundless over time, thereby rendering the zero state response inconsequential. To be sure, practical circuits do not produce time domain responses that tend toward infinity in the limit of progressively larger times. But large outputs in physically realizable passive and active circuits can, at worst, result in catastrophic circuit failure. At best, they dramatically deteriorate circuit linearity. In either event, unstable realizations of presumably linear circuits are undesirable in that they are incapable of producing zero state responses that relate linearly to applied signal excitations.

A final noteworthy case is conditional stability, for which there exists at least one pole such that

$$Re(2s_i) = 0. \quad (1-54)$$

Equation (1-54) is satisfied for either a real pole whose value is zero or for a conjugate imaginary pole pair, say $(2s_i5 6jv)$. For $(2s_i)5 0$, a component of the first term on the right hand side of (1-51) gives rise to a constant component of the net output response. On the other hand, $(2s_i)5 6jv$ can be shown to imply two terms in the first function on the right hand side of (1-51) that produce a sinusoidal component to the zero input response. In either case, the net...
output response does not ultimately reduce to a time domain function that mirrors the required signal processing criteria. The second case is particularly troublesome in that it compromises an unstable resonance condition\[8\]. Unstable circuit resonance is a theoretically boundless net circuit response that is generated when the input signal is itself a sinusoid whose radial frequency matches the magnitude of the imaginary part of a complex conjugate pole pair having zero real part.

1.4.1. LAPLACE TRANSFORM

The zero state and the zero input responses of a linear circuit containing energy storage elements derive from an exploitation of KVL and/or KCL, which produce integro-differential equations of equilibrium. The derivation and solution of these time domain equations can be simplified, and analytical insights can be correspondingly enhanced, by applying KVL and/or KCL to a frequency domain model of the linear circuit at hand, instead of to the actual circuit whose branch volt ampere characteristics are formulated in the time domain. The mathematical tool that paves the way to replacing time domain analyses by purely algebraic considerations in the frequency domain is the Laplace transform\[9\].

The Laplace transform, \( F(s) \), of a time domain function, \( f(t) \), is

\[
F(s) = \int_{0}^{\infty} f(t) e^{-st} dt \quad L[f(t)],
\]

(1-55)

where \( s \), termed the Laplace variable or complex frequency, is the complex number,

\[
s = s + jv.
\]

(1-56)

Since time \( t \) is the integration variable on the right hand side of (1-55), and limits of \( t \to 0 \) and \( t \to \infty \) are invoked subsequent to integrating the integrand, \([f(t)e^{st}]\), \( F(s) \) is exclusively a function of the Laplace variable, \( s \). In order for the time domain function to be Laplace transformable, there must exist a value of \( s \), such that

\[
\int_{0}^{\infty} \left| f(t) e^{-st} \right| dt < \infty.
\]

(1-57)

Not all functions are Laplace transformable. But all time domain functions pertinent to the analysis and design of linear circuits and systems do have Laplace transforms. Tables of such transforms are ubiquitous in the basic circuits and systems literature\[10\].

When applied to the linear circuit of Fig. (1.38), analysis in the frequency domain entails the replacement of the time domain signal source function, \( x_s(t) \), by its Laplace transform, \( X_s(s) = L[x_s(t)] \). In concert with this substitution, the time domain response, \( y(t) \), is
supplanted by its Laplace transform, \( Y(s) = \mathcal{L}[y(t)] \), where

\[
Y(s) = Y_{zi}(s) + Y_{zs}(s) .
\]  
(1-58)

In this relationship, \( Y_{zi}(s) \) symbolizes the Laplace transform of the time domain zero input response, and \( Y_{zs}(s) \) is the Laplace transform of the time domain zero state response.

![Symbolic Depiction Of The Frequency Domain Model Of The Linear System Abstracted In Fig. (1.38).](image)

In order for the transformed response to relate meaningfully to both the transformed input function and the initial conditions imposed by the energy storage elements of the circuit, the circuit itself in Fig. (1.38) must be appropriately transformed into an equivalent frequency domain structure. Such a transformation, which is symbolically illustrated in Fig. (1.39), means that all time domain branch voltages, branch currents, and node voltages are replaced by their respective Laplace transforms. But care must be exercised during this transformation process because the branch voltage appearing across, and the branch current flowing through, an element are interrelated by the electrical nature of the branch element. Fortunately, only two special transformations cases prevail. These are (1) an exclusively algebraic volt ampere relationship for a branch element and (2) a branch element volt ampere characteristic that involves a time derivative of either a branch voltage or a branch current.

### 1.4.1.1. ALGEBRAIC VOLT AMPERE RELATIONSHIP

Algebraic volt ampere relationships are pervasive of linear resistors, linear conductors, and the four types of linear controlled sources investigated earlier. For example, Ohm's law defines the volt ampere characteristics of the linear resistor diagrammed in Fig. (1.40a) as

\[
V_R(t) = R \cdot I_R(t) .
\]  
(1-59)

From (1-55) the transform, \( V_R(s) \), of the resistor branch voltage is

\[
V_R(s) = \int_{0}^{\infty} V_R(t) e^{-st} \, dt = \int_{0}^{\infty} R \cdot I_R(t) e^{-st} \, dt .
\]

Since \( R \) is a constant, independent of time,
\[ V_R(s) = R \int_0^t i_R(t) e^{-st} dt = R I_R(s). \]  

Equation (1-60) implies that a resistance in the time domain remains a resistance in the frequency domain, as depicted in Fig. (1.40b). Implicit to this assertion is the understanding that the time domain branch voltage, \( v_R(t) \), developed across the resistance and the time domain branch current, \( i_R(t) \), flowing through the resistance are replaced by their frequency domain, Laplace transforms, \( V_R(s) \) and \( I_R(s) \), respectively.

Analogous conclusions apply to all four types of linear controlled sources, since the controlling parameter, like the resistance treated above, is time invariant. Thus, for example, a VCCS has \( i(t) \) \( 5 g_m v(t) \) in the time domain. In the frequency domain, this branch element is the companion equation, \( I(s) \) \( 5 g_m V(s) \), where \( I(s) \) is the Laplace transform of the controlled time domain current, \( i(t) \), and \( V(s) \) is the transform of the time domain controlling voltage, \( v(t) \).

1.4.1.2. TIME DERIVATIVE VOLT AMPERE RELATIONSHIP

Volt ampere relationships involving first order time derivatives of voltages or currents are encountered in linear capacitors and linear inductors. The development of the frequency domain model for both of these energy storage elements exploits the general fact that the Laplace transform of the first derivative of a time domain function, \( f(t) \), is

\[ L \left[ \frac{df(t)}{dt} \right] = sF(s) - f(0^+) \]  

where \( F(s) \) is the Laplace transform of \( f(t) \), and \( f(0^+) \) represents the initial (immediately after the application of input energy at time \( t = 0 \)) value of the function, \( f(t) \).

The application of (1-61) to the volt ampere characteristic,
\[ i_C(t) = C \frac{d}{dt} v_C(t), \]  

(1-62)

of the linear capacitor offered in Fig. (1.41a) produces

\[ I_C(s) = sC \left[ V_C(s) - \frac{v_C(0^+)}{s} \right], \]  

(1-63)

where \( I_C(s) \) is the Laplace transform of the time domain branch current, \( i_C(t) \), flowing through the capacitor, \( V_C(s) \) is the Laplace transform of the time domain voltage, \( v_C(t) \), developed across the linear capacitor, and \( v_C(0^+) \) represents the voltage to which the capacitor is initially charged. Since voltages across linear capacitors subjected to finite time domain currents are incapable of instantaneous changes, the voltage, \( v_C(0^+) \), immediately after the application of a circuit input, is identical to the voltage, \( v_C(0^-) \), immediately prior to input excitation. It follows that (1-63) is replaceable by the slightly more convenient expression,

\[ I_C(s) = sC \left[ V_C(s) - \frac{v_C(0^-)}{s} \right], \]  

(1-64)

A circuit level interpretation of (1-64) derives from the observation that its mathematical form is reminiscent of the simple volt ampere relationship of a linear conductance, which is, of course, a memoryless circuit element. In particular, the term, \( sC \), might be viewed as the "complex conductance" of a linear, uncharged capacitor that supports a frequency domain voltage given by the bracketed term on the right hand side of (1-64). In the frequency domain capacitor model postulated in Fig. (1.41b), note that the voltage developed across the uncharged capacitance is precisely the bracketed term in question. The fact that this net voltage appears in associated reference polarity with the frequency domain capacitive current, \( I_C(s) \), supports the contention of an analogy between (1-64) and the simple Ohm's law relationship that relates the current flowing through a linear conductance to the voltage developed across the conductance.

![Fig. (1.41).](image)
The Frequency Domain. There Is No Initial Charge Associated With The Capacitor Represented By C In This Model.

The "complex conductance" alluded to in the preceding paragraph is the admittance, \( Y_C(s) \), of the linear, uncharged capacitor. Accordingly, with \( Y_C(s) D sC \), (1-64) becomes

\[
I_C(s) = Y_C(s) \left[ V_C(s) - \frac{V_C(0^+)}{s} \right].
\]

(1-65)

Equivalently,

\[
V_C(s) = \frac{V_C(0^+)}{s} + Z_C(s) I_C(s),
\]

(1-66)

where

\[
Z_C(s) = \frac{1}{Y_C(s)} = \frac{1}{sC}
\]

(1-67)

is the impedance of the linear, uncharged capacitance. It should be noted that KVL applied to the frequency domain capacitor model of Fig. (1.41b) yields (1-66), provided that the capacitor is perceived in the frequency domain as a "complex resistance," or impedance, of \( 1/sC \).

\[\text{Fig. (1.42). (a). A Linear Inductor In The Time Domain. An Initial Current, } i_L(0^-), \text{ Flows Through The Inductor With the Reference Direction Indicated In The Diagram. (b). The Linear Inductor Of (a) Modeled In The Frequency Domain. There Is No Initial Current Associated With The Inductor Represented By L In This Model.}\]

Results that are similar to the foregoing disclosures are obtained for the linear inductor of Fig. (1.42a), whose time domain volt ampere characteristic is

\[
v_L(t) = L \frac{d i_L(t)}{dt}.
\]

(1-68)
Using (1-61) and the fact that currents flowing through inductors stressed by bounded voltages are incapable of instantaneous change, it is a simple matter to show that the frequency domain interpretation of (1-68) is

\[ V_L(s) = sL \left[ I_L(s) - \frac{i_L(0^2)}{s} \right] - Z_L(s) \left[ I_L(s) - \frac{i_L(0^2)}{s} \right], \]

(1-69)

where \( Z_L(s) = \frac{1}{sL} \) is the impedance of an inductor that conducts no initial current. Equivalently, (1-69) can be written as

\[ I_L(s) = \frac{i_L(0^2)}{s} \left[ 1 - Y_L(s) V_L(s) \right], \]

(1-70)

with

\[ Y_L(s) = \frac{1}{Z_L(s)} = \frac{1}{sL} \]

(1-71)

representing the admittance of an inductor supporting zero initial current flow. The circuit level interpretation of both (1-69) and (1-70) in the frequency domain is given in Fig. (1.42b).

1.4.2. FREQUENCY DOMAIN CIRCUIT ANALYSIS

If the linear circuit illustrated symbolically in the time domain in Fig. (1.38) and in the frequency domain in Fig. (1.39) is of order \( n \), \( n \) initial conditions can be assigned independently to the energy storage elements embedded in the circuit. In the frequency domain, each of these initial conditions is either a voltage source in series with an inactive capacitor (i.e. a capacitor with no initial voltage) or a current source in shunt with an inactive inductor. Assuming that the independent source of energy, \( x_s(t) \), is applied to the linear circuit at time \( t = 0 \), the value of each initial condition source is of the form, \( \frac{G_k(0^2)}{s} \), where \( G_k(0^2) \) is the voltage established across a capacitor or the initial current flowing through an inductor, immediately before the application of the input independent source.

The frequency domain volt ampere characteristics of each branch of an \( n \)th order linear circuit are algebraic relationships of the form of (1-60), (1-63), or (1-69), which are, in general, functions of the complex frequency, \( s \). It follows that the Laplace transform of the zero input response of such a circuit is an algebraic superposition of the effects of each \( \frac{G_k(0^2)}{s} \). In particular,

\[ Y_{zi}(s) = \sum_{k=1}^{n} G_k(s) \left[ \frac{G_k(0^2)}{s} \right], \]

(1-72)

where \( G_k(s) \), which is independent of all \( G_k(0^2) \), is the proportionality constant linking the \( k \)th initial condition source to the branch or node variable that is the zero input response. This proportionality constant quantifies the impact exerted on the zero input response by the \( k \)th
initial condition. It derives from an application of KVL and KCL to the circuit at hand, and it is a function of \( s \), owing to the algebraic nature of the frequency domain volt ampere relationships of each branch of a linear circuit. It should be clearly understood that (1-72) is the Laplace transform of the time domain zero input response defined by (1-50); that is,

\[
Y_{zi}(s) = \sum_{k=1}^{n} G_k(s) \left[ \frac{G_k(0^2)}{s} \right] \left\{ \sum_{i=1}^{n} k_i e^{2s_i t} \right\},
\]

(1-73)

Just as the transformed zero input response is the linear superposition of the effects of each transformed initial condition source, the zero state response is the linear superposition of the effects of all transformed independent inputs. In the network of Figs. (1.38) and (1.39), there is only one independent source of energy. Thus,

\[
Y_{zs}(s) = H_s(s) X_s(s),
\]

(1-74)

where \( H_s(s) \) is termed the transfer function of the linear circuit. The transfer function is the proportionality constant that links the transformed source to the transformed output variable of a linear circuit. Since the complete response of a linear circuit is the sum of the zero input and zero state responses, the transformed complete response is expressible as

\[
Y(s) = Y_{zs}(s) + Y_{zi}(s) = H_s(s) X_s(s) + \sum_{k=1}^{n} G_k(s) \left[ \frac{G_k(0^2)}{s} \right] \left\{ \sum_{i=1}^{n} k_i e^{2s_i t} \right\}.
\]

(1-75)

For a linear, \( n \)th order, lumped circuit modeled in the frequency domain, the transfer function, \( H_s(s) \) in (1-74) is always a ratio of real polynomials in the Laplace variable, \( s \). Algebraically, \( H_s(s) \) is of the form

\[
H_s(s) = \frac{K A(s)}{B(s)},
\]

(1-76)

where \( K \) is a constant, independent of \( s \), and \( B(s) \) is an \( n \)th order polynomial whose roots are the circuit poles, \( (2s_i) \), appearing in (1-50) and discussed in Section (1.4.0). Thus,

\[
B(s) = \prod_{s_1, s_2} \left( s - s_1 s_2 \right),
\]

(1-77)

and

\[
B(2s_1) = 0;
\]

(1-78)

that is, the roots of the so called characteristic polynomial,

\[
B(s) = 0,
\]

(1-79)
are the poles of the linear circuit that appear in (1-50). In general, \( A(s) \) is the \( z \)th order polynomial, 

\[
A(s) = \prod_{p=1}^{z} \left( s + s_p \right),
\]

where \( z < n \) and \((2s_p)\), which is the \( p \)th root of \( A(s) \), is termed the \( p \)th zero of the transfer function. Unlike the poles of a linear circuit, the asymptotic stability of a linear circuit is not necessary precluded if the real part of \((s_p)\) is zero or negative. But like the poles, any \((s_p)\) that is a complex number is matched by a companion zero that is the complex conjugate of \((s_p)\).

The proportionality constants, \( G_k(s) \), in (1-75) are also ratios of real polynomials in \( s \). The roots of the denominator polynomials of \( G_k(s) \) are identical to the roots of the characteristic polynomial of the linear circuit, but the zeros associated with \( G_k(s) \) are not necessarily the same as the roots of \( A(s) \) in (1-80). Thus, \( G_k(s) \) is expressible as

\[
G_k(s) = K_k \frac{A_k(s)}{B(s)},
\]

(1-81)

where \( K_k \) is a constant,

\[
A_k(s) = \prod_{p=1}^{z_k} \left( s + s_p^{(k)} \right),
\]

(1-82)

and \( z_k^{(k)} \) is not necessarily equal to \( z \) but is always less than or equal to \( n \). Moreover, the roots of \( A_k(s) \), which are implicitly defined by the equation,

\[
A_k(s) = 0,
\]

are not necessarily the same as the zeros associated with the transfer function of the circuit.

Since the circuit of Fig. (1.39) is linear, the transfer function, \( H_s(s) \), is independent of the transformed input excitation, \( X_s(s) \). The initial condition proportionality functions, \( G_k(s) \), are likewise invariant with the \( G_k(0) \). These facts allow setting \( X_s(s) \) and the \( G_k(0)/s \) to convenient frequency domain values that expedite the calculation of \( H_s(s) \) and the \( G_k(s) \). For example, consider setting all \( G_k(0)/s \) to zero, which reflects a consideration of only the zero input response. Additionally, if \( X_s(s) \) is set to one, (1-75) implies a net transformed response of

\[
Y(s) = G_0(s) 0 \left[ \frac{Y_{zs}(s)}{X_s(s)} \right] 5 \frac{H_s(s)}{s}.
\]

(1-84)

This result states that the net transformed response, under the conditions of unity input and
zero initial conditions, is the transfer function of the circuit. Since a frequency domain signal of one is the Laplace transform of the unit impulse time domain function, \( d(t) \), the inverse transform of the frequency domain response corresponding to the excitation conditions that lead to (1-84) is termed the impulse response, \( h_s(t) \), of the circuit. Specifically,

\[
h_s(t) = L^{-1} \left\{ Y(s) : G_f(0^2) = G_f(0^2,0) \right\} = L^{-1} \left\{ H_s(s) \right\}.
\]

(1-85)

The circuit level implications of the preceding two relationships are illustrated symbolically by Fig. (1.43).

![Diagram](image)

**Fig. (1.43).** Time And Frequency Domain Interpretations Of The Unit Impulse Response Of A Linear Circuit With Memory. Note That The Unit Impulse Response Is Formally Defined For Only Zero State Conditions.

The proportionality functions, \( G_k(s) \), can be found in a fashion that mirrors the methodology underlying the determination of \( H_s(s) \). In particular, consider setting \( X_s(s) = 0 \), which corresponds to zero input signal excitation in the time domain. From (1-75), the resultant transformed zero input response reduces to \( G_k(s) \) if for all \( i \neq k, G_i(0^2)/s = 0 \) and \( G_k(0^2)/s = 1 \). Physically, this analytical tack means that all initial states, except the \( k \)th, are sequentially nulled and additionally, the frequency domain value of the \( k \)th initial condition source is replaced by a value that represents the Laplace transform of the unit impulse.
function.
1.4.2.1. **FIRST ORDER PASSIVE CIRCUIT EXAMPLE**

As a first illustration of frequency domain circuit analysis techniques, consider the low pass RC filter depicted in Fig. (1.44a), for which the signal source voltage, \( v_s(t) \), is the step function,

\[
v_s(t) = E u(t),
\]

shown in Fig. (1.44b). The output voltage, \( v_o(t) \), is to be determined under the condition that the capacitor, \( C \), in this circuit is initially charged to a voltage of \( V_{\text{cap}} \), with the polarity indicated in the circuit.

Fig. (1.45a) depicts the frequency domain model of the circuit in Fig. (1.44a). The time domain step function voltage source defined by (1-86) has been replaced by its Laplace transform, \( E/s \), and the capacitive branch has been modeled in accordance with (1-66) and Fig. (1.41b). Since only one independent signal source and one initial condition prevails, the transformed zero state response, say \( V_{\text{OZS}}(s) \), is generated by a single source of independent energy \( E/s \), and the transformed zero input response, say \( V_{\text{OZI}}(s) \), is likewise attributed to only a single energy source \( (V_{\text{cap}}/s) \). The transformed net response, \( V_o(s) \), is therefore expressible as

\[
V_o(s) = V_{\text{OZS}}(s) H_s(s) + V_{\text{OZI}}(s) = \frac{E}{s} \left( 1 + G_c(s) \right) \frac{V_{\text{cap}}}{s}.
\]

Fig. (1.45b) contains the circuit pertinent to computing the transfer function, \( H_s(s) \), in (1-87) is submitted in Fig. (1.45b). Note that the transformed signal source is supplanted by a frequency domain value of one and that the transformed initial condition voltage associated with the capacitor is set to zero. The transfer function is the voltage divider,
\[
H_s(s) = \frac{1}{R_1 C} \frac{1}{s + 1},
\]
which can be written as
\[
H_s(s) = \frac{1}{R_1 C} \frac{1}{s + \frac{1}{R_1 C}},
\]
\[(1-88)\]

Fig. (1.45). (a). Frequency Domain Model Of The low pass RC Filter Given In Fig. (1.44a). (b). Frequency Domain Model Used To Compute The Transfer Function Of The low pass RC Filter. (c). Steady State Time Domain Model Of The low pass RC Filter. (d). Frequency Domain Model Used To Compute The Proportionality Function Linking The Capacitor Initial Condition Voltage To The Zero Input Circuit Response.

where
The time constant of the first order circuit is

\[ t = R_1 C, \]  

(1-89)

Before proceeding further, several points in regard to the foregoing calculations warrant emphasis. First, the circuit at hand is of first order and thus, the transfer function of (1-88) displays but a single pole. More precisely, (1-88) suggests the first order characteristic polynomial in \( s \),

\[ B(s) = s + \frac{1}{t} = 0, \]  

(1-90)

whose single solution, \( s = -\frac{1}{t} \), defines the pole of the first order circuit. Second, note that the Thévenin resistance, say \( R_{\text{thc}} \), seen by the capacitor, \( C \), in the circuit of Fig. (1.45b) is the parallel combination of the resistances, \( R_1 \) and \( R_2 \). It follows that (1-89) can be written as

\[ t = R_{\text{thc}} C. \]  

(1-91)

Equation (1-91) is a general result applicable to all first order, linear, capacitive circuits. The analogous time constant for all first order, linear, inductive circuits is

\[ t = \frac{L}{R_{\text{thl}}}, \]  

(1-92)

where \( R_{\text{thl}} \) represents the Thévenin resistance facing the inductance, \( L \), in the zero state frequency domain model of the first order inductive configuration. The single pole at \( s = -\frac{1}{t} \) is a general result applicable to all first order linear circuits.

A third critical point is that the time constant, \( t \), of the circuit undergoing study is positive for physically realizable, and hence positive and real, \( R_1 \), \( R_2 \), and \( C \). Since, \( t > 0 \), the circuit pole at \( -\frac{1}{t} \) lies in the left half of the complex frequency plane, and the circuit is therefore asymptotically stable. All first order circuits that contain no dependent current or voltage sources are asymptotically stable.

Returning to the problem of evaluating the zero state response, (1-87) and (1-88) yield

\[ V_{\text{ozs}}(s) = \frac{E/R_1 C}{s(s + \frac{1}{t})}. \]

A partial fraction expansion (also known as a Heaviside expansion) of this result, followed by the use of (1-89), leads to
The inverse Laplace transform of (1-93) is the time domain zero state response for time \( t > 0 \):

\[
V_{\text{ozs}}(t) = 5 \left( \frac{R_2}{R_2 1 R_1} \right) \mathcal{E} \left( \frac{1}{s 2} \frac{1}{s 1 \frac{1}{t}} \right).
\]  

(1-94)

Observe that \( v_{\text{ozs}}(0^+) = 0 \). This result reflects engineering expectation, since for zero state operating conditions, the capacitor in the circuit of Fig. (1.44a) is uncharged. But since a capacitor is incapable of instantaneous voltage changes for finite circuit excitations, the voltage, \( v_{\text{ozs}}(0^+) \), appearing across the capacitor immediately after an application of the input signal source must remain zero.

Observe further that in the steady state,

\[
V_{\text{ozs}}(\infty) = 5 \left( \frac{R_2}{R_2 1 R_1} \right) \mathcal{E}.
\]  

(1-95)

This operating circumstance confirms the low pass nature of the circuit by demonstrating its ability to "pass" zero frequency input signals to its output port; that is, the filter provides a non-zero zero state response to zero, and thus low, frequency inputs. This low pass characteristic is also understandable in light of the fact that the input signal applied to the circuit in Fig. (1.44a) is a constant for time \( t > 0 \). Since the circuit in question is linear, all responses, inclusive of the zero state output voltage, \( v_{\text{ozs}}(t) \), must ultimately collapse to constants that are linearly related to the constant input voltage. But since the output voltage is extracted directly across the capacitor, the steady state, or ultimate, constant current flowing through the capacitance must be zero. Zero current flowing through any branch element is tantamount to an open circuited branch. If the capacitive branch in Fig. (1.44a) is indeed open circuited, the network reduces to the structure offered in Fig. (1.45c), which suggests the voltage divider expression in (1-95).

Fig. (1.45d) is the circuit appropriate to the determination of the proportionality function, \( G_c(s) \), in (1-87). This topology derives from Fig. (1.45a), except that the transformed signal source is nulled, and the transformed initial condition voltage is replaced by one. With the help of (1-89), circuit analysis produces

\[
G_c(s) = 5 \left( \frac{R_1 \left| R_2 \right|}{R_1 \left| R_2 1 \frac{1}{sC} \right|} \right) s \frac{s}{s 1 \frac{1}{t}}.
\]  

(1-96)

From (1-87), the transformed zero input response is
\[ V_{ozi}(s) = \frac{V_{\text{cap}}}{s(1/t)} \]

whence, a time domain zero input response of

\[ V_{ozi}(t) = V_{\text{cap}} e^{t/t} \]  

(1-97)

Note that the time domain zero input response ultimately vanishes, as is always the case for asymptotically stable circuits. The superposition of (1-94) and the preceding result leads to the complete time domain response,

\[ v_o(t) = \left( \frac{R_2}{R_2 + R_1} \right) e^{2t/t} \left( 1 + \frac{1}{e^{2t/t}} \right) + V_{\text{cap}} e^{t/t} \]  

(1-98)

![Graph showing zero state, zero input, and net time domain responses.](image)

Fig. (1.46). Zero State, Zero Input, And Net Time Domain Responses For The Low-pass Filter Of Fig. (1.44a). The Input Signal Is A 9 Volt Amplitude Step, And The Capacitor Is Initially Charged To 22 Volts. The Branch Element Parameters Are \( R_2 = 2R_1 = 3 \) KV And \( C = 1 \) nF.
which confirms that $v_o(0^+) = V_{\text{cap}}$, as stipulated in the original statement of the problem. Moreover, $v_o(\cdot ) = 0$, as anticipated.

Fig. (1.46) graphically portrays the time domain nature of (1-98), along with its constituent zero state and zero input components for the case of $R_1 = 1.5$ kV, $R_2 = 3$ kV, $C = 1$ nF, $E = 9$ volts, and $V_{\text{cap}} = 22$ volts. These branch element parameters yield $t = 1 \text{ mSEC}$ and

$$
\left( \frac{R_2}{R_1 + R_2} \right) E = 6 \text{ volts}.
$$

The responses depicted in Fig. (1.46), and particularly, the zero state response shown in the graph, suggest sluggish responsiveness of the low pass network. This sluggishness is a consequence of the fact that the capacitor in Fig. (1.44a), across which the output voltage response is developed, inherently resists rapid fluctuations of its terminal voltage. Several figures of merit are commonly used to quantify the relative response speed of a low pass circuit. One of the more popular of these figures of merit is the rise time, $T_{\text{rise}}$, which is the time required for the zero state response to a step input excitation to proceed from 10% -to- 90% of its final, or steady state, value, as illustrated in Fig. (1.47). Using (1-93), it is easy to show that

$$
T_{\text{rise}} = t_{90} - t_{10} = 2.2t.
$$

Thus, for small $t$, which requires minimal capacitance and/or minimal Thévenin resistance seen by the capacitance, $T_{\text{rise}}$ is small. In turn, a small $T_{\text{rise}}$ implies an ability of the filter to respond quickly to the instantaneous change in input voltage effected by the application of the step source signal.

1.4.2.2. SECOND ORDER PASSIVE CIRCUIT EXAMPLE

A second illustration of frequency domain analysis techniques is afforded by an examination of the second order, low pass $RLC$ filter depicted in Fig. (1.48a). Embedded in this circuit are two energy storage elements: an inductor of inductance $L$, whose initial current (in the polarity direction indicated) is $I_{\text{ind}}$, and a capacitor of capacitance $C$, whose initial voltage (also in the indicated polarization) is $V_{\text{cap}}$. For the purpose of this study, assume that the signal source voltage, $v_s(t)$, whose internal Thévenin resistance is $R$, is the step of amplitude $E$ defined by (1-86) and that the total output response is the voltage, $v_o(t)$. 
Fig. (1.47). Zero State Response For The low pass Filter Of Fig. (1.44a). The Input Signal Is A 9 Volt Amplitude Step, And The Branch Element Parameters Are $R_2 = 2R_1 = 3 \text{ KV}$ And $C = 1 \text{ nF}$. The Plot Introduces Rise Time As A Figure Of Merit For Gauging The Speed Of Response Of A low pass Filter.
As usual, $v_o(t)$ is the superposition of a zero state response, $v_{o zs}(t)$, and a zero input response, $v_{o zi}(t)$. But while $v_{o zs}(t)$ is the ramification of only one source of energy, $v_s(t)$, $v_{o zi}(t)$ is the linear superposition of the effects of both the initial inductor current and the initial capacitor voltage. It follows that in transformed frequency variables, $V_o(s)$ is of the form,
where the transfer relationships, $H_s(s)$, $G_c(s)$, and $G_l(s)$ are the transformed output voltages delineated in the frequency domain models of Figs. (1.48b), (1.48c), and (1.48d), respectively. It should be clear that the first term on the right hand side of (1-100) is the transformed zero state response, while the sum of the last two terms on the right hand side of (1-100) defines the transformed zero input response.

A straightforward application of KVL and KCL to the frequency domain model of Fig. (1.48b) delivers a transfer function, $H_s(s)$, given by

$$H_s(s) = \frac{\frac{1}{LC}}{s^2 + \frac{R}{L}s + \frac{1}{LC}}.$$  

This expression can be cast in the canonical form,

$$H_s(s) = \frac{V_n^2}{s^2 + 2zv_n s + v_n^2},$$

where $v_n$, termed the undamped natural frequency of oscillation of the second order circuit, is

$$v_n = \frac{1}{\sqrt{LC}},$$

and

$$2zv_n = \frac{R}{L}.$$  

In (1-104) $z$, the damping factor of the circuit, can be related to circuit parameters in accordance with

$$z = \frac{R}{2v_n L} = \frac{R}{2} \frac{\sqrt{C}}{L}.$$  

Using (1-103) and (1-105), an analysis of the structures of Figs. (1.48c) and (1.48d) delivers

$$G_c(s) = \frac{s(s + 2zv_n)}{s^2 + 2zv_n s + v_n^2}.$$
\[ G_1(s) = \frac{s/C}{s^2 + 2zv_n s + v_n^2}. \]  

(1-107)

The insertion of (1-102), (1-106) and (1-107) into (1-100) leads to a transformed zero state response, \( V_{ozs}(s) \), of

\[ V_{ozs}(s) = \frac{v_n^2 E}{s^2 + 2zv_n s + v_n^2}, \]  

(1-108)

and a transformed zero input response, \( V_{ozl}(s) \), of

\[ V_{ozl}(s) = \frac{s^2 + 2zv_n s + v_n^2}{s^2 + 2zv_n s + v_n^2} \]  

(1-109)

The inverse Laplace transform of the preceding two frequency domain relationships yields the time domain zero state and zero input responses. The execution of these inverse transformations is complicated by the fact that the order of the characteristic polynomial,

\[ B(s) = s^2 + 2zv_n s + v_n^2 = 0, \]  

(1-110)

is two. Its roots, say \( s_1 \) and \( s_2 \) (the poles of the circuit), which are

\[ s_1, s_2 = -zv_n \pm jv_d, \]  

(1-111)

are therefore real, multiple real, or complex, depending on whether \( z \) is greater than one, equal to one, or less than one, respectively. The discussion that follows addresses only the so called underdamped case of \( z < 1 \), for this operational situation is commonly encountered in the design-oriented analysis of electronic circuits and systems. The overdamped case of \( z > 1 \) and the critically damped case of \( z = 1 \) are left as exercises for the student.

For the underdamped case of less than unity damping factor \( (z < 1) \), (1-111) shows that the two poles of the circuit are the complex conjugate pair,

\[ s_1, s_2 = -zv_n \pm jv_d, \]  

(1-112)

where

\[ v_d = \sqrt{1 - 2z^2} \]  

(1-113)

defines the damped natural frequency of oscillation for the circuit at hand. The resultant time
domain zero state response, $v_{ozs}(t)$, which is the inverse Laplace transform of the right hand side of (1-108) is, for time $t \geq 0$\cite{12},

$$
v_{ozs}(t) = E \left( 1 + \frac{e^{2zv_n t}}{\sqrt{12z^2}} \right) \left[ \sin \left( v_{d}t \cos^2 z \right) \right].
$$

(1-114)

Since

$$
\sin \left( \cos z \right) = \sqrt{12z^2},
$$

(1-115)

(1-114) confirms that $v_{ozs}(0^+) = 0$, which is as expected, since the capacitor, across which the output voltage is extracted, is presumed initially uncharged for the zero state response. For $zv_n = 0$, (1-114) shows that $v_{ozs}() = E$. This result is also no surprise since for a constant input signal, all branch voltages and branch currents, including the capacitor voltage and the inductor current in the RLC circuit of Fig. (1.48a), ultimately reduce to constants. But constant inductor current corresponds to zero voltage across the inductor (thereby lending credence to the popular statement that "inductors are short circuits for DC"). On the other hand, constant capacitor voltage implies zero capacitor current ("capacitors are open circuits for DC"). Resultantly, $v_{ozs}()$ in Fig. (1.48a) is identical to $v_s()$, which is, of course, the constant, $E$.

Although the zero state response to step excitation of the second order low pass filter in Fig. (1.48a) converges to its anticipated steady state value of $E$, it is oscillatory about $E$, as the normalized curves in Fig. (1.49) illustrate. The radial frequency of these oscillations is the damped frequency of oscillation, $v_d$. Although these oscillations decay with time because the circuit undergoing study has $zv_n = 0$, the response displays periodic overshoot and undershoot. Note in Fig. (1.49), particularly for small damping factor, that the slope, $dv_{ozs}(t)/dt$, of the zero state response is periodically zero at values of $v_{ozs}(t)$ that are larger and smaller than $E$. The maximum overshoot, which occurs at the first value of positive time for which $dv_{ozs}(t)/dt = 0$, can be substantial, depending on the value of the damping factor, $z$. For example, $z = 0.2$ yields a maximum overshoot of almost 53%.

When step inputs, or at least rapidly changing signal levels are applied to second order active systems in which sensitive electronic devices are embedded, the large response overshoots caused by severe underdamping can catastrophically damage devices. Even if electronic devices do not fail, the repeated application of such inputs induces thermal stresses within them. The potential cumulative effect of these stresses is an impairment of the long term operating reliability of the electronic system. At best, underdamped second order active and passive networks faithfully emulate rapidly changing inputs only when steady state operation nominally prevails. Unfortunately, progressively longer times are required to approximate the steady state as $z$ diminishes. The upshot of the matter is that although underdamped circuits tend to respond faster than their overdamped or critically damped counterparts, underdamping in the amount of $z$ less than about 0.7 is a serious drawback in
such applications as stereo systems, radio and television receivers, radar detectors, and many other electronic circuits and systems.

A dramatic illustration of the effects of severe underdamping in the circuit of Fig. (1.48a) is afforded by the extreme case of $z = 0$. From (1-114), $z = 0$ gives a zero state response of

$$v_{ozs}(t) = \frac{5}{1 + 2 \sin(v_n t)},$$

which is a sinusoid, offset by $E$ volts, whose radial frequency is the undamped (undamped, because $z = 0$) natural frequency of oscillation, $v_n$. The zero damping case results in non-

---

Fig. (1.49). Time Domain Zero State Response To Step Excitation Of The Second Order Filter Shown In Fig. (1.48a). The Vertical Scale Plot Is Normalized To The Amplitude Of The Input Step, Thereby Effectively Yielding A Plot Of The Unit Step Response. The Horizontal, Or Time, Scale Is Normalized To The Inverse Of The Undamped Natural Frequency Of Oscillation Of The Filter.
asymptotically stable behavior, since the input step signal produces a sinusoidal response that
never converges to the anticipated steady state value of \( E \). The circuit functions as an oscillator.

To be sure, an oscillator cannot be realized by passive components alone. For example, in the
filter of Fig. (1.48a), (1-105) shows that \( z < 0 \) requires \( R > 0 \), which is impossible with practical
interconnective wiring. But active circuits, particularly active circuits that exploit feedback
signal paths from output -to- input ports, can produce negative resistances that effectively
cancel physical resistances in selected circuit branches, thereby rendering zero damping a
plausible operating condition.

Having discussed and obtained the zero state response to step excitation of the
second order RLC filter of Fig. (1.48a), the complete time domain output voltage, which is the
superposition of the zero state and zero input responses, requires an inverse Laplace
transformation of (1-109). This inverse transformation delivers a zero input response, \( v_{ozi}(t) \), of

\[
 v_{ozi}(t) = \frac{V_{\text{cap}} e^{\frac{2}{\sqrt{12}} z v_{n} t}}{\sqrt{12 z^2}} \sin \left[ v_{d1} t \tan^{-1} \left( \frac{\sqrt{12} z^2}{z} \right) \right]
 + \frac{I_{\text{ind}} e^{\frac{2}{\sqrt{12}} z v_{n} t}}{v_{d} C} \sin \left( v_{d} t \right).
\]

(1-117)

Observe that both the capacitive and the inductive components of the zero input response
have the damped sinusoidal form indigenous to the transient component of the zero state
response given by the second term on the right hand side of (1-114). Thus, like the zero state
output, the zero input response of an underdamped second order circuit displays undershoot
and overshoot. Moreover, the zero input response, which, it must be remembered, is the
output in the absence of an externally applied input, is an eternal sinusoid if \( z < 0 \). Oscillators
used in radio and television receivers have no explicit input. They produce sinusoidal
oscillations at a radial frequency, \( v_{n} \), by relying on the ability of circuit turn on transients to
initialize the energy storage elements of the circuit.

Fig. (1.50) completes the analytical investigation of the circuit of Fig. (1.48a) by
displaying time domain plots of the zero state, zero input, and net output responses. For
plotting purposes, \( R \) is taken to be 50 ohms, \( L = 1 \text{ mH} \), \( C = 250 \text{ pF} \), \( E = 5 \text{ volts} \), \( V_{\text{cap}} = 5 \text{ volts} \), and
\( I_{\text{ind}} = 20 \text{ mA} \). The values for \( R \), \( L \), and \( C \) yield a damping factor, \( z \), of 0.395, an undamped
natural frequency of oscillation, \( v_{n} \), of 2\( p(10.07 \text{ Mhz}) \), and a damped frequency of oscillation, \( v_{d} \),
of 2\( p(9.25 \text{ Mhz}) \).

**EXAMPLE (1.9)**

Reconsider the circuit of Fig. (1.15a), but for simplicity, assume that \( R_{1} = R_{2} \), \( D = R \) and \( C_{1} = C_{2} \), \( D = C \). The resultant schematic diagram and its equivalent time domain
circuit are depicted in Fig. (1.51), where \( v_{i} \) symbolizes the input signal and \( v_{o} \) is the
output signal.. Determine the transfer function, \( H_{i}(s) \), of the network. Use this
transfer relationship to find allowable values of the gain parameter, \( k \), such that
asymptotically stable circuit behavior is ensured. Additionally, find the range of \( k \)
commensurate with a critically damped response.
The Zero State, Zero Input, And Complete Responses For The Circuit Of Fig. (1.48a). The Circuit Has $R = 50 \, \text{V}$, $L = 1 \, \text{mH}$, And $C = 250 \, \text{pF}$. The Input Signal Is A Step Of Amplitude 3 Volts, The Capacitor Is Charged Initially to 25 Volts, And The Inductor Conducts An Initial Current Of 20 mA.

**SOLUTION (1.9)**

The transfer function derives from a simple nodal analysis conducted in the frequency domain. Because the transfer function pertains to only the zero state response of a circuit, the capacitors may be tacitly presumed to be initially at rest.
Fig. (1.51). (a). Active, Second Order, Low Pass Filter Examined In EXAMPLE (1.9). (b). Equivalent Circuit Of The Structure In (a). The Amplifier, Whose Voltage Gain Is \( k \), Is Assumed To Draw No Input Current; that is, \( i_x = 0 \) in (a).

1. KCL applied at the node where \( V_y(s) \) is developed gives

\[
\frac{V_y(s) - V_1(s)}{R} + \frac{V_y(s) - V_x(s)}{R} + sC \left[ V_y(s) - V_o(s) \right] = 0.
\]

The transformed voltage, \( V_x(s) \), relates to its transformed counterpart, \( V_y(s) \), by the simple voltage divider expression,

\[
V_x(s) = \left( \frac{1/sC}{R + 1/sC} \right) V_y(s) = \frac{V_y(s)}{1 + sR C}.
\]

The combination of these two expressions, along with the fact that

\[
V_o(s) = kV_x(s),
\]
leads to

\[ H_s(s) = \frac{V_o(s)}{V_i(s)} = \frac{k/(RC)^2}{s^2 + \left(\frac{32k}{RC}\right)s + \left(\frac{1}{RC}\right)^2} \]

(2). The denominator of the transfer function reveals the characteristic polynomial,

\[ s^2 + \left(\frac{32k}{RC}\right)s + \left(\frac{1}{RC}\right)^2 = 0, \]

which is of the standard form,

\[ s^2 + 2zv_n s + v_n^2 = 0. \]

Hence, the undamped natural frequency of the circuit (in units of radians per second) is

\[ v_n = \frac{1}{RC} \]

and the damping coefficient is

\[ z = \frac{32k}{2}. \]

(3). For asymptotic stability, \( z \) must be greater than zero. It follows that asymptotic stability mandates \( k < 3 \). On the other hand, critical damping corresponds to \( z = 1 \), whence \( k \) must be less than or equal to one to achieve critically damped responses.

Observe that the voltage amplifier allows the low pass filter to be oscillatory, as is the case for \( k \neq 3 \).

1.4.3. STEADY STATE SINUSOIDAL ANALYSIS

A broadly exploited class of input signals for linear circuits and systems is the sinusoidal function,

\[ x_s(t) = X_m \cos(vt + f), \]

(1-118)

where \( X_m, f, \) and \( v \) respectively represent the amplitude, phase angle (in radians), and frequency (in radians per second) of the sinusoid. Two fundamental reasons underlie the importance of (1-118) to electronic circuits and systems. First, many systems are driven by sinusoids or by signals that can be represented by a superposition of sinusoids. For example,
the signal transmitted by a radio station and ultimately detected by a radio receiver is sinusoidal. The frequency, \( \nu \), of the transmitted signal, which is the frequency to which the radio must be tuned for proper reception, is called the carrier frequency. In amplitude modulated (AM) communication systems, the amplitude, \( X_m \), of the transmitted carrier is varied as a linear function of the numerical data or audio information that is to be communicated, while \( \nu \) is held constant. In frequency modulated (FM) systems, \( X_m \) is held fast, and \( \nu \) is varied in proportion to the communicated information. Even the information detection mechanism within a radio is predicated on a sinusoid that is internally generated by a circuit called the local oscillator. In accordance with the preceding example, the local oscillator is a second order active circuit designed expressly for zero damping coefficient.

Circuit testing comprises a second justification for the sinusoid. In particular, it is far easier to design a circuit that generates a good approximation of a perfect sinusoidal signal than it is to design a circuit that outputs a reasonable approximation of a step function, impulse function, ramp (or saw tooth) or any other waveform. Moreover, it is significantly easier to measure the amplitude and phase angle of a sinusoidal signal than it is to measure the zero state, zero input, and complete responses of circuits excited by non-sinusoidal inputs. Fortunately, much of the information implicit to the complete response of a circuit can be extracted from a comparison of the steady state sinusoidal response of a circuit to the sinusoidal signal applied to that circuit. The network analyzer, a commonly available piece of laboratory equipment used to characterize circuit performance over broad ranges of signal frequencies, exploits this measurement fact.

### 1.4.3.1. Phasors

Let the sinusoidal signal defined by (1-118) be applied to the symbolic circuit of Fig. (1.52). As usual, the resultant output consists of a zero input component and a zero state component or equivalently, a transient and a steady state component. If the circuit is asymptotically stable, the zero input and transient response components ultimately disappear, thereby leaving only a steady state response. Since all responses in a linear circuit must ultimately reflect the time domain nature of the input signal, this steady state response is necessarily a sinusoid\textsuperscript{[13]}. Thus, the resultant steady state response, \( y_{ss}(t) \), of the circuit in Fig. (1.52) is of the form,

\[
y_{ss}(t) \xrightarrow{D} \lim_{t \to \infty} y(t) = 5 Y_s \cos(\nu t + \phi)
\]

(1-119)
It is important to understand that although the amplitude, $Y_s$, and the phase angle, $u$, of the steady state sinusoidal response are likely to differ from the corresponding parameters, $X_s$ and $f$, respectively, of the input sine wave, the output signal frequency, $v$, is identical to the frequency of the input sinusoid.

The complete and steady state sinusoidal responses of a linear circuit can certainly be obtained through an application of the Laplace techniques discussed in the preceding section of material. But if attention is focused on only the steady state response to applied sinusoidal excitation, network phasors are a more convenient analytical tool. Phasor methods of analysis are applicable only to linear circuits driven by sinusoidal voltages and currents. They exploit the fact that in the steady state, a linear, sinusoidally driven circuit produces a sinusoid of precisely the same frequency as the frequency of the applied excitation. Moreover, phasor methods produce meaningful analytical results only when they are used in conjunction with asymptotically stable networks. In these circuits, the zero input and transient responses incurred by an application of a sinusoidal signal at time $t = 0$ eventually vanish to ensure an observable steady state sinusoidal response.

The definition of a phasor derives from Euler's identity:
\[
e^{jC} = \cos C + j\sin C.
\] (1-120)

When applied to (1-118), this identity allows the alternative expression for $x_s(t)$,
\[
x_s(t) = \text{Re}\left[X_s e^{jvt}\right],
\] (1-121)
where $\text{Re}[b]$ symbolizes the mathematical operation of computing the "real part of $b$." Equation (1-21) can be rewritten as
\[
x_s(t) = \text{Re}\left(X_s(jv) e^{jvt}\right),
\] (1-122)
where
\[
X_s(jv) = X_s e^{jf}
\] (1-123)
represents the phasor of $x_s(t)$. The phasor of $x_s(t)$ is seen to be a complex number. Its magnitude is the amplitude, and its phase is the phase angle, of the time domain sinusoid it represents. Despite the notation, $X_s(jv)$, which suggests that the phasor of $x_s(t)$ is functionally dependent on the frequency of $x_s(t)$, phasors never convey any information in regard to frequency. Frequency is arguably a superfluous variable in steady state investigations of linear circuits driven by sinusoids because the frequency of the steady state output sinusoid is identical to that of the applied input sinusoid. Nevertheless, the notation in question is retained as a convenient way of keeping track of the numerical value of the input signal.
frequency. Thus, for example, the phasor of a 5 volt sinusoid whose frequency is 800 radians per second and whose phase angle is 308 (or \( \pi/6 \) radians) is written

\[
X_s(j 800) = 5 e^{j \pi/6} \text{ volts.}
\]

In similar fashion, the steady state response, \( y_{ss}(t) \), can be written as

\[
y_{ss}(t) = \Re \left[ Y_s e^{j \omega t + \phi} \right],
\]

whence the phasor of \( y_{ss}(t) \) is

\[
Y_{ss}(j \omega) = Y_s e^{j \phi}.
\]

1.4.3.2. FREQUENCY AND PHASE RESPONSES

A study of the steady state sinusoidal response of a linear circuit reveals much of the circuit characterization information conveyed by the zero state, zero input, and complete responses to step or impulsive inputs. A steady state investigation entails the measurement of the frequency response and the phase response of the circuit under test.

The measurement of the frequency response begins with the application of an input sinusoid of known amplitude, frequency, and phase angle, as shown in Fig. (1.52). With the input signal amplitude, \( X_s \), held fast, the amplitude, \( Y_s \), of the steady state sinusoidal response is measured as the input signal frequency, \( \omega \approx 2\pi f \), is varied over a specified range of values. The frequency response is a plot of the output signal amplitude-to-input signal amplitude ratio, \( Y_s/X_s \), which is termed the gain of the circuit, versus \( \omega \) (in radians per second) or \( f \) (in hertz). Because \( \omega \) is typically varied over several decades, the frequency response is generally displayed in semi-logarithmic form, with \( \omega \) placed on the logarithmic axis. The linear vertical axis of the frequency response is plotted either as the ratio, \( Y_s/X_s \), or the value of this ratio in decibels (dB), where

\[
\frac{Y_s}{X_s} \text{ (in dB)} = 20 \log_{10} \left( \frac{Y_s}{X_s} \right).
\]

A zero dB value of gain implies \( Y_s / X_s \), a negative dB value corresponds to \( Y_s / X_s \), and a positive dB value corresponds to \( Y_s / X_s \).

For fixed input signal amplitude, the amplitude of the resultant sinusoidal output signal is determined by the circuit undergoing investigation. Accordingly, the frequency response defines the ability of a network to process input signals over a range of frequencies. For example, if \( Y_s/X_s \) is constant for \( 0 < \omega \), the circuit is known as an all pass network, since the circuit under test is able to process all input signal frequencies uniformly. On the other hand, if the gain of the circuit is relatively constant at low frequencies, but diminishes to zero
for very large \( v \), the circuit is a low pass structure; that is, it efficiently processes low signal frequencies, but it is unable to sustain constant gain at high signal frequencies. Band pass circuits deliver nominally constant gain over a narrow frequency interval. Outside this interval, the gain attenuates toward zero. Finally, high pass circuits deliver a nominally constant \( Y_s/X_s \) ratio at high frequencies, but their gain at low frequencies reduces to zero.

The measurement of the phase response of a linear circuit proceeds in a fashion that is identical to the measurement of the frequency response, except that instead of measuring the output signal amplitude, the phase angle, \( \mu \), is monitored as a function of input signal frequency. The phase response is a plot of the phase difference, \( \mu 2 f \), between sinusoidal output and sinusoidal input signals, -versus- signal frequency \( v \) (or \( f \)). Like the frequency response, the phase response is plotted on semi-logarithmic graph paper.

The phase response is indicative of the time required for the input signal to propagate through the circuit under test; that is, it is a measure of the signal delay incurred by the circuit. This assertion is validated by writing (1-119) in the form

\[
y_{ss}(t) = Y_s \cos\left[ v\left( t + \frac{\mu}{v} \right) \right].
\]  

(1-127)

Since in general, the function, \( \cos\left[ v\left( t + T \right) \right] \), is a cosine waveform delayed (shifted to the right in the time domain plot of the waveform) by \( T \) seconds, (1-127) suggests an output steady state sinusoid delayed by the amount, \( 2(\mu/v) \). It follows that the signal delay, say \( \tau_d(v) \), incurred by the circuit is

\[
\tau_d(v) = 2\left( \frac{\mu 2 f}{v} \right).
\]  

(1-128)

Phase distortion refers to the situation in which signals at varying frequencies are delayed non-uniformly. Zero phase distortion, which is an idealized performance attribute, therefore requires a phase response that decreases linearly with the signal frequency, \( v \). It is appropriate to interject that since the signal delay given by (1-128) is not defined for \( v = 0 \), the signal delay is often supplanted by the envelope delay, \( \tau_d(v) \), which is given by

\[
\tau_d(v) = 2\left( \frac{d(\mu 2 f)}{dv} \right).
\]  

(1-129)

Note that \( \tau_d(v) = \tau_d(v) \) if the phase difference, \( \mu 2 f \), is a linear function of the signal frequency, \( v \).

The frequency and phase responses are intimately related to the transfer function concept introduced earlier. To underscore this relationship, represent the time domain sinusoid applied to the circuit of Fig. (1.52) as the phasor defined by (1-123), and let the corresponding steady state response be represented by the phasor of (1-125). The situation at hand is diagrammed in Fig. (1.53). It is understood that if the circuit of Fig. (1.52) is asymptotically stable, all initial capacitor voltages and inductor currents can be set to zero in
the process of formulating the steady state frequency domain model used in Fig. (1.53). Thus, the circuit in Fig. (1.53) is effectively in its zero state, which implies that the ratio of the output phasor -to- the input phasor is related to the transfer function, \( H_s(s) \), introduced in (1-84). Specifically,

![Diagram](https://via.placeholder.com/150)

**Fig. (1.53). Steady State Sinusoidal Investigation Of The Circuit In Fig. (1.52).**

\[
\frac{Y_{ss}(\mathbf{v})}{X_s(\mathbf{v})} = 5 \left( \frac{Y_s}{X_s} \right) e^{j(\omega f)} 5 H_s(s); \ s \ 5 \ (s \ 1 \ jv). \]

That is, the output -to- input phasor ratio in the network of Fig. (1.53) is the transfer function of the network, with the Laplace variable, \( s \), replaced by the imaginary variable, \( jv \). Recall from (1-85) that the impulse response, \( h_s(t) \), of a circuit is the inverse Laplace transform of the circuit transfer function, \( H_s(s) \), where in general, \( s \ 5 \ (s \ 1 \ jv) \). Then, by (1-57), the substitution, \( s \ 5 \ jv \) is tantamount to stipulating that

\[
\int_0^\infty e^{2st} \left| h_s(t) \right| dt, \quad \text{for} \ s \ 5 \ 0.
\]

The transfer function, \( H_s(jv) \), or the input -to- output gain, as it is often referred to, pertinent to the steady state sinusoidal response of a linear, asymptotically stable circuit is obviously a complex number. The plot, \(-versus- \omega\), of the magnitude, \( Y_s/X_s \), of this complex number is the frequency response of the circuit, and the plot, also \(-versus- \nu\), of the phase angle of \( H_s(jv) \) is the phase response of the circuit. Although \( H_s(jv) \) can be evaluated by first determining \( H_s(s) \) and then replacing the variable, \( s \), by \( jv \), \( H_s(jv) \) can be found directly through an appropriate application of KVL and KCL to the circuit of interest. In addition to the presumption of asymptotic stability, this application of KVL and KCL embodies the following constraints and guidelines.

(1) The circuit undergoing investigation must be excited only by sinusoids. If more than one sinusoid is applied to the circuit, linearity allows for an exploitation of superposition principles. In the case of multiple inputs, whose individual phasors are \( X_i(jv) \), several transfer functions, say \( H_i(jv) \), are determined to evaluate the resultant
output phasor, \( Y_{ss}(jv) \), as

\[
Y_{ss}(jv) = H_1(jv) X_1(jv) + H_2(jv) X_2(jv) + H_3(jv) X_3(jv) + \ldots. \tag{1-131}
\]

(2). The presumption of asymptotic stability implies a zero input response that vanishes in the steady state. Since attention is focused on only steady state circuit performance, the initial conditions imparted on circuit capacitors and inductors can be arbitrarily set to zero.

(3). The steady state frequency domain volt ampere characteristic of a circuit branch resistor, similar to that diagrammed in Fig. (1.40a) is

\[
V_R((jv)) = R I_R(jv), \tag{1-132}
\]

where \( V_R(jv) \) and \( I_R(jv) \) respectively denote the phasor of the voltage developed across, and the phasor of the current flowing through, the resistor of resistance, \( R \).

(3). With \( s \) replaced by \( (jv) \), the steady state volt ampere characteristic of the capacitor diagrammed in Fig. (1.41a) is

\[
I_C((jv)) = jvC V_C(jv), \tag{1-133}
\]

where \( V_C(jv) \) and \( I_C(jv) \) respectively denote the phasor of the voltage developed across, and the phasor of the current flowing through, the capacitor of capacitance, \( C \). The imaginary quantity, \( (jvC) \), is termed the admittance of the capacitor, while the inverse, \( (1/jvC) \), of this imaginary number is the impedance of the capacitor. Similarly, for the inductor of Fig. (1.42a),

\[
V_L((jv)) = jvL I_L(jv), \tag{1-134}
\]

where \( (jvL) \), symbolizes the impedance of the inductor. The inverse, \( (1/jvL) \), of this imaginary number is the admittance of the inductor.

1.4.3.3. FIRST ORDER CIRCUIT EXAMPLE

A demonstration of the utility of steady state frequency domain analytical methods is afforded by a reconsideration of the low pass RC filter depicted in Fig. (1.44a), for which the signal source voltage, \( v_s(t) \), is assumed to be a cosine waveform. The impedance, say \( Z_2(jv) \), of the parallel combination of the resistance, \( R_2 \), and the capacitor, \( C \), is

\[
Z_2(jv) = R_2 \left| \frac{1}{jvC} \right| 5 R_2 \left( \frac{1}{jvC} \right) + \frac{1}{1/jvC} \cdot \frac{R_2}{1} \cdot \frac{R_2}{jvR_2C} = \frac{R_2}{1} \cdot \frac{R_2}{jv \cdot R_2C}. \tag{1-135}
\]
Equation (1-135) predicts a shunting output port impedance that approaches $R_2$ for zero frequency ($v \approx 0$). For very large signal frequencies ($v \gg 0$), (1-135) predicts a short circuited output port branch, in that $Z_2(jv) \approx 0$. Both of these conclusions are reasonable. In the first case, a zero frequency input corresponds to a constant input signal, since the applied excitation is a cosine function. In the steady state, capacitors in networks activated by constant voltages or currents behave as open circuits. The parallel combination of $R_2$ and an open circuit is obviously $R_2$. For the case of infinitely large signal frequency, which implies an infinitely large rate of change in the applied (finite) cosine signal, the output voltage developed across the capacitor cannot change instantaneously. Therefore, this voltage cannot track the input signal, and the capacitor effectively behaves as a short circuit. In turn, the parallel combination of $R_2$ and an effective short circuit is the short circuit itself; that is, it is zero ohms.

The transfer function of the circuit at hand is now seen to be the voltage divider,

$$H_s(jv) = \frac{Z_2(jv)}{Z_2(jv) + R_1} = \frac{R_2}{R_2 + R_1} \frac{1}{1 + jv R_1 C}.$$  \hspace{1cm} (1-136)

Recalling from (1-89) that the circuit time constant, $t$, is $(R_1|R_2)C$, (1-136) can be written in the form,

$$H_s(jv) = \frac{1}{1 + \frac{1}{jv R_1 C}},$$

which is identical to the $s \approx jv$ value of (1-88).

The frequency and phase responses implied by (1-136) are depicted in Fig. (1.54). The frequency response plot is normalized to the zero frequency value, $H_s(j0)$, of the transfer function. This is to say that the frequency response in Fig. (1-54) plots the magnitude of the function,

$$H_n(jv) = \frac{H_s(jv)}{H_s(j0)} = \frac{1}{11 \frac{1}{jv t}}.$$

Since $H_s(j0)$ is a real positive number, which therefore has zero phase angle associated with it, the phase angle, $\phi(v)$, of $H_s(jv)$ is the same as the phase angle of the normalized transfer characteristic, $H_n(jv)$; namely,

$$\phi(v) = 2 \tan^{-1} (vt).$$  \hspace{1cm} (1-138)

Assuming that the input sinusoid has zero reference phase angle, the plot, shown in Fig. (1.54), of the phase angle - versus $v$ defines the phase response of the RC filter at hand.

Just as figures of merit, such as the rise time and the percentage overshoot,
quantify circuit performance attributes in terms of the time domain responses to step excitation of linear circuits, so are figures of merit invoked to assess circuit quality directly in terms of steady state frequency domain response to a sinusoidal inputs. Among the most common of the frequency domain figures of merit used to assess high speed circuit performance capabilities is the 3-dB bandwidth, say $B_{3dB}$. In low pass circuits the 3-dB bandwidth in radians -per- second is the value of signal frequency for which the magnitude of the transfer function at $\nu = B_{3dB}$, $|H_s(jB_{3dB})|$, is three decibels smaller than the
magnitude of the zero frequency value of the transfer function. Since three decibels corresponds to a numerical value of $\sqrt{2}$, $B_{3dB}$ is implicitly defined by the constraint,

$$|H_s(jB_{3dB})| = 5 \left| \frac{H_s(j0)}{\sqrt{2}} \right|.$$  

(1-139)

In view of the fact that the normalized transfer relationship of (1-137) has a zero frequency value of one, (1-139) applied to (1-137) gives

$$\left| \frac{1}{1 + \frac{B_{3dB}}{t}} \right| = 5 \left| \frac{1}{\sqrt{1 + \left(\frac{B_{3dB}}{t}\right)^2}} \right| 5 \frac{1}{\sqrt{2}}.$$
It follows that the 3-dB bandwidth of the circuit in Fig. (1.44a) is

\[ B_{3dB} = \frac{1}{t} \]  \hspace{1cm} (1-140)

Thus, the 3-dB bandwidth of the RC structure under investigation is the inverse of the circuit time constant. Since the circuit rise time is proportional to the circuit time constant, which is, in turn, the negative inverse of the circuit pole, \( B_{3dB} \) conveys much of the same type of circuit performance information that is conveyed by an interpretation of circuit analysis results formulated in the time domain.

1.4.3.4. SECOND ORDER CIRCUIT EXAMPLE

Equation (1-102) gives the transfer function of the second order, low pass RLC network of Fig. (1.48a). For steady state sinusoidal circuit analysis, this transfer relationship is

\[ H_s(j\omega) = \frac{1}{1 + \left(\frac{\omega}{\omega_n}\right)^2 + j2\zeta\left(\frac{\omega}{\omega_n}\right)} \]  \hspace{1cm} (1-141)

Observe that \( H_s(j0) = 1 \), which reflects the facts that the inductor in the circuit at hand is a steady state short circuit for constant (zero frequency) input excitation, and the capacitor is a steady state open circuit for constant inputs. Accordingly, the gain function in (1-141) is, in this case, also equal to the normalized gain function,

\[ H_n(j\omega) = \frac{H_s(j\omega)}{H_s(j0)} \]  \hspace{1cm} (1-142)

Fig. (1.55) displays the frequency response implied by the normalized transfer function, \( H_n(j\omega) \), of a generalized second order, low pass circuit operated under various conditions of underdamping. Fig. (1.56) is the corresponding phase response. These graphs, which are plotted against the normalized frequency, \( \omega/\omega_n \), reveal several interesting trademarks of underdamped, second order circuits and systems.

First, unlike the situation that prevails in first order low pass networks, the frequency response of an underdamped, second order, low pass configuration is not necessarily a monotonically decreasing function of signal frequency. In particular, response peaking is evidenced for small damping coefficients. The non-zero frequency, say \( \omega_p \), at which such peaking occurs can be determined by equating the first frequency derivative of \( H_s(j\omega) \) in (1-141) to zero. The result is

\[ \frac{\omega_p}{\omega_n} = \sqrt{1 + 2\zeta^2} \]  \hspace{1cm} (1-143)
and the corresponding peaked value of the normalized response, say $m_p$, is

$$m_p = \frac{D}{H_n(z_p)} \cdot \frac{1}{2z \sqrt{1 - z^2}}.$$

Interestingly, $v_p$ in (1-143) is an imaginary number if $z > 1/\sqrt{2}$; that is, frequency response peaking prevails only for imaginary values of the input signal frequency. But since imaginary radial signal frequencies do not exist, the implication of $z > 1/\sqrt{2}$ is that no peaking of the frequency response is possible. Equivalently, the frequency response given by (1-141) for the special case of $z > 1/\sqrt{2}$ is a monotonically decreasing function of frequency, as suggested by the curves in Fig. (1.55). For $z < 1/\sqrt{2}$, $m_p$ in (1-142) is one. Recalling the monotone decreasing
nature of the frequency response for $z > 1/\sqrt{2}$ and the fact that $H_s(j0) \leq 1$, $z \leq 1/\sqrt{2}$, for which $m_p \leq 1$, implies that the frequency response in question is constant or flat for a broad range of signal frequencies. The constraint, $z \leq 1/\sqrt{2}$, is a commonly invoked criterion in the design of low pass, wide band electronic circuits and systems. This design objective stems from the fact that a flat frequency response is indicative of an ability to process all input signal frequencies with uniform gain.

Another significant feature of underdamped second order circuits surfaces through a consideration of the special case of a signal frequency that is numerically equal to the undamped natural frequency of oscillation, $\nu_n$. From (1-141) and (1-142), the normalized gain function at $\nu = \nu_n$ is
\[
H_n(jv_n) = \frac{1}{j2z}.
\]

(1-145)

The transfer function, \(H_n(jv_n)\), is imaginary, with a phase angle of \((2908)\), as depicted in Fig. (1.56). Moreover, \(H_n(jv_n)\) is infinitely large if \(z = 0\), which means that theoretical steady state output signal amplitude generated in response to a sinusoidal input is unbounded. The zero damped circuit is non-asymptotically stable since, as discussed earlier, zero damping is commensurate with the production of sinusoidal oscillations in both the zero state and the zero input responses to step or impulse excitations. The zero damped circuit is, in fact, conditionally stable, in the sense that an input sinusoid whose frequency matches the undamped natural frequency of oscillation results in an unbounded steady state output signal.

Finally, the 3-dB bandwidth, \(B_{3dB}\), can be determined for the second order circuit by applying (1-139) to the transfer function of (1-141). Such an application results in the requirement,

\[
\left[\frac{1}{2} \left(\frac{B_{3dB}}{v_n}\right)^2\right]^2 + 4z^2 \left(\frac{B_{3dB}}{v_n}\right)^2 = 2,
\]

whose positive solution is

\[
B_{3dB} = \frac{v_n}{2} \left[\frac{1}{2} z^2 + 1 \sqrt{11 + \left(\frac{1}{2} z^2\right)^2}\right]^{1/2}.
\]

(1-146)

Observe that for \(z = \sqrt{2}\), the condition for a flat frequency response, the 3-dB bandwidth is numerically equal to the undamped natural frequency of oscillation.

1.5.0. REFERENCES