Problem #05:

In an attempt to inspire design interest and to foster design intuition, this problem, as well as the subsequent problem, focuses on the design, as well as the computer-based confirmation of the adequacy of the design, of the two stage series-shunt feedback amplifier addressed definitively in class. The basic schematic diagram of the subject circuit appears in Fig. (P5a), where the two active devices are understood to be the silicon-germanium (SiGe) bipolar junction transistors whose SPICE parameters are provided in conjunction with Problem #02. The two power supply voltages, $V_{CC}$ and $V_{EE}$, are each 2.7 volts. On the other hand, the battery voltage, $V_{IQ}$, symbolizes the quiescent operating voltage at the input port of the amplifier. This latter voltage is zero if the amplifier serves as the first stage of an electronic system but in general, it is the quiescent output port voltage of a predecessor stage in the system. The transistors deliver nearly optimal gain-bandwidth product when their static collector currents ($I_{cQ}$) are approximately 1.6 mA and their static collector-to-emitter voltages ($V_{ceQ}$) are numerically equal to roughly twice the quiescent value of the base-to-emitter biasing voltage ($V_{beQ}$). Recall from the preceding assignment that $V_{beQ} \approx 820$ mV when $I_{cQ} = 1.6$ mA and $V_{ceQ} \approx 1.6$ volts. Recall further that at this operating point, the static base-to-collector current gain is $h_{FE} \approx 107$. For a signal source resistance, $R_s$, of 300 $\Omega$, the amplifier is to deliver a closed loop small signal voltage gain, $A_{vc}$, of 10, or 20 dB.

![Schematic Diagram](image)

(a). In contrast to the implications of discussions contained in most electronics textbooks, the
biasing requirements are rarely independent of the desired small signal operating constraints. To this end, show that if the transistors in the schematic diagram of Fig. (P5a) conduct negligible static base currents and conduct quiescent emitter currents of $I_{eQ}$, corresponding to a base-emitter bias level of $V_{beQ}$, and if transistor $Q2$ supports a collector-emitter voltage of $2V_{beQ}$, resistance $R_2$ must be selected in accordance with

$$R_2 = \frac{(A_{vc} - 1)V_{EE} + A_{vc}V_{iQ} - (A_{vc} + 2)V_{beQ}}{I_{eQ}}.$$ 

Then, demonstrate that resistance $R_1$ satisfies the relationship

$$R_1I_{eQ} = V_{EE} + \left(\frac{A_{vc}}{A_{vc} - 1}\right)V_{iQ} - \left(\frac{A_{vc} + 2}{A_{vc} - 1}\right)V_{beQ}.$$ 

(b). Design the amplifier so that each transistor conducts nominal collector currents ($I_{cQ}$) of 1.6 mA and supports nominal collector-emitter voltages of $2V_{beQ}$. Assume $V_{iQ} = 0$. Calculate the quiescent voltage, with respect to ground, at each circuit node. Record these voltages so that you can ultimately test the propriety of your design with the static results predicted by a SPICE simulation of the circuit. [You should arrive at approximate resistance values of $R_{c1} \approx 1160 \, \Omega$, $R_{c2} \approx 560 \, \Omega$, $R_1 \approx 990 \, \Omega$, and $R_2 \approx 8940 \, \Omega$.]

(c). Simulate the circuit on SPICE.

(i). Compare the SPICE operating point results with the computed static node voltages, and adjust appropriate circuit parameters as required.

(ii). Examine the simulated small signal gain at low signal frequencies. You will likely observe a simulated gain that is considerably smaller than the gain value of 20 dB for which the circuit was designed. This difference derives largely from analyses that tacitly ignore both the internal series emitter and Early resistances of the transistors. Recall, for example, that the nominal emitter resistance of the SiGe devices is almost 14 $\Omega$, which is hardly the traditional small value that can be ignored. Rectify the situation at hand by replacing resistance $R_{c2}$ by an ideal current source whose value is precisely the static current that $R_{c2}$ conducts in the designed circuit. Current sources, and particularly ideal ones, are hard to come by, but we shall examine this problem in due time. For now, assume that ideal current sources are available so that the circuit in Fig. (P5a) modifies to the structure given in Fig. (P5b). Re-simulate the small signal frequency response. Your low frequency gain should now be well within 15% of the designed value of 10, or 20 dB.

(iii). For the circuit in Fig. (P5b), record the simulated low frequency gain, $A_{vc}(0)$, 3-dB bandwidth, $B_{vc}$, and the unity gain frequency, $\omega_{uc}$.

(d). Show analytically that if a lowpass amplifier has a single left half plane pole at a frequency of $s = -p_{vc}$, the 3-dB bandwidth is $B_{vc} = p_{vc}$, and the unity gain frequency is approximately, $\omega_{uc} \approx A_{vc}(0)p_{vc} = A_{vc}(0)B_{vc}$. Is the amplifier in Fig. (P5b) a dominant pole amplifier? In other words, can its frequency response be approximated by the response implied by a single pole lowpass network?

**Problem #06:**

You have doubtlessly found that the amplifier in Fig. (P5b) is not a dominant pole circuit. Non-dominant pole circuits are the proverbial kiss of death in electronic sys-
tems since they are potentially stable entities and at best, they give rise to transient responses having unacceptable overshoots and settling times. Let us examine the possibility of correcting this problem by adding a compensation capacitor, $C_c$, across the base-emitter terminals of transistor $Q2$, as depicted in Fig. (P6).

(a). Choose $C_c = 100 \text{ fF}$, and use SPICE to examine the small signal frequency response and in particular, the zero frequency gain, the 3-$dB$ bandwidth, and the unity gain frequency. If the amplifier exudes a nominally dominant frequency response, its unity gain frequency should be within 5% of the gain-bandwidth product. Is the amplifier a dominant pole circuit? If it is not, increase $C_c$ in about 20 fF increments until the desired pole dominant response is obtained. For the finalized circuit, what is the low frequency gain, $A_{vc}(0)$, 3-$dB$ bandwidth, $B_{vc}$, and the unity gain frequency, $\omega_{uc}$? Recalling the answers to Part (d) of the preceding problem, what prices are paid for dominant pole compensation?

(b). Modify the circuit in Fig. (P6) so that you can use SPICE to simulate directly the open loop voltage gain, say $A_{vo}$. As a hint, consider how the feedback imposed on the circuit can be nulled for signal purposes without affecting the quiescent operating conditions. What are the SPICE predictions of open loop low frequency gain and open loop 3-$dB$ bandwidth, $B_{vo}$? Calculate the loop gain and show that the closed loop 3-$dB$ bandwidth is larger than its open loop counterpart by roughly a factor of one plus the loop gain.

(c). Use the small signal model to calculate the time constant associated with the compensation capacitance, $C_c$. How does the inverse of this time constant compare to the open loop 3-$dB$ bandwidth? Why is this inverse time constant not precisely equal to the simulated open loop 3-$dB$ bandwidth?

(d). Use SPICE to simulate the driving point input impedance, $Z_{iin}$, seen by the signal source. Plot the frequency responses of the real and imaginary parts of this impedance. Is the input port inductive or capacitive within the 3-$dB$ passband of the amplifier?

(e). Use SPICE to simulate the driving point output impedance, $Z_{out}$, seen at the output port. Plot the frequency responses of the real and imaginary parts of this impedance. Is the output port inductive or capacitive within the 3-$dB$ passband of the amplifier?

Problem #07:
Fig. (P7) depicts a so-called shunt-series feedback amplifier. The currents, $I_{iQ}$ and $I_{oQ}$, are bias current levels, $I_i$ is input signal current, and $I_{os}$ is the signal component of net output current. In the analytical inquiries that follow, ignore internal emitter and collector resistances, and assume that the transistor Early resistances are sufficiently large to justify their tacit neglect.

(a). What subcircuit in the amplifier comprises the feedback subcircuit? Is the input port of this subcircuit connected in series or shunt with the input port of the amplifier? Is the output port of this subcircuit connected in series or shunt with the output port of the amplifier?

(i). Based on the foregoing observations, what type of two-port parameters are most suitable for modeling the feedback subcircuit? Find these two port parameters and draw the two-port equivalent circuit of the feedback structure.

(ii). Do you expect the input impedance of the amplifier to be increased or diminished by the feedback subcircuit? Do you expect the output impedance of the amplifier to be increased or diminished by the feedback subcircuit? Accordingly, is the amplifier best suited for use as a voltage amplifier, a current amplifier, a transconductor, or a transimpedance amplifier?

(b). Use the small signal model of the utilized bipolar transistors to deduce the following performance barometers:

(i). the open loop gain;
(ii). the closed loop gain;
(iii). the loop gain;
(iv). the open loop and closed loop input resistance seen by the signal source;
(v). the open loop and closed loop output resistances seen by the effective load element, $R_{c2}$.

Fig. (P7)
Problem #05: