Problem #08:

In the CMOS common source amplifier shown in Fig. (P8), the devices are biased to operate in their respective saturation regimes. Since one transistor is an NMOS unit while the other is PMOS, it is unreasonable to presume that the values of corresponding small signal parameters are identical. Moreover, channel length modulation and bulk-induced perturbation of threshold voltage cannot be ignored in either device. Assume, however, that the only significant capacitances in the circuit are those that are expressly delineated in the schematic diagram.

(a). Use the MOS technology small signal model to deduce an expression for the low frequency small signal voltage gain, $A_v = V_o/V_s$.

(b). Repeat Part (a), but evaluate the low frequency small signal input and output resistances, $R_{in}$ and $R_{out}$, respectively.

(c). Use the small signal model to evaluate the time constants associated with the capacitances, $C_i$ and $C_o$.

(d). In light of the gate-source, gate-drain, drain-bulk, and source-bulk capacitances indigenous to MOSFETs, what transistor capacitances must reasonably be included with each of the circuit capacitances identified as $C_i$ and $C_o$?

(e). If $R_s$ is a relatively small Thévenin source resistance, what capacitance establishes the dominant pole of the circuit, what is the frequency of this dominant pole, and what is the approximate resultant gain-bandwidth product?

(f). What inequality must be satisfied by $R_s$ if the amplifier at hand is to emulate a dominant pole frequency response characteristic with a phase margin of nominally $65^\circ$?
Problem #09:

Repeat all parts of Problem #08 for the alternative CMOS amplifier depicted in Fig. (P9).

Problem #10:

In the gain-enhanced common gate amplifier shown in Fig. (P10), the devices are biased to operate in their respective saturation regimes. Do not presume that the values of the corresponding small signal parameters for the two transistors are identical. Moreover, channel length modulation phenomena can be tacitly ignored, but bulk-induced perturbation of threshold voltage must be considered. Assume, however, that the only significant capacitances in the circuit are those that are expressly delineated in the schematic diagram.

(a). Use the MOS technology small signal model to deduce an expression for the low frequency small signal current gain, \( A_i = I_{os}/I_s \). The current, \( I_Q \), is a biasing current.
b. Repeat Part (a), but evaluate the low frequency small signal input and output resistances, $R_{in}$ and $R_{out}$, respectively.

c. Use the small signal model to evaluate the time constants associated with the capacitances, $C_i$ and $C_o$.

d. In light of the gate-source, gate-drain, drain-bulk, and source-bulk capacitances indigenous to MOSFETs, what transistor capacitances must reasonably be included with each of the circuit capacitances identified as $C_i$ and $C_o$?

e. What capacitance most likely establishes the dominant pole of the circuit, and what is the frequency of this dominant pole?

f. What conditions must be satisfied if the amplifier at hand is to emulate a dominant pole frequency response characteristic with a phase margin of nominally $65^\circ$?

**Problem #11:**

The circuit offered in Fig. (P11) is a commonly used topology for the generation of sinusoidal oscillations in communication system applications. The oscillation frequency, as well as the condition for generating oscillatory behavior is determined by the undamped natural frequency and damping factor of the net effective load impedance imposed differentially across the drain terminals of the two transistors (which operate in saturation). Use the small signal MOSFET model to determine the conditions that underlie the initiation and maintenance of sinusoidal oscillations. Also, determine the steady state frequency of oscillation. For simplicity, channel length modulation phenomena can be ignored.

![Circuit Diagram](image)
Problem #08: