1. Course Description

This course covers computer organization and design. It provides CS/CE/EE students with a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), and branch prediction are also discussed. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Students design in Verilog and use ModelSim simulator to verify their RTL design/simulation exercises.

2. Learning Objectives

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design. This course is also expected to improve students’ design skills and analytical skills.

3. Course administration

a) Course prerequisites: EE354L (previously EE254L or EE201L) Introduction to Digital Circuits is a necessary prerequisite. Undergraduate students without this prerequisite will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

Recommended Preparation: Familiarity with the following items at an introductory level is expected.

1. Programming in an assembly language of any processor (CISC or RISC)
2. Digital Logic design at RTL level (Register Transfer Language Level)
3. Design entry using Verilog HDL (Hardware Description Language) and simulation
b) Classes:  http://classes.usc.edu/term-20163/classes/ee-457

Discussion class is not optional. The homeworks and the lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) Examinations:  No makeup exams.

Please check to see if you have any conflict (personal or academic) and bring it to my attention via email to gandhi@usc.edu within the first three weeks of classes. **If you have not brought it to my attention by 9/12/2016, I assume that you are completely in agreement with these dates and times. No late requests for any accommodation will be considered. Occasionally students may have a class conflict. Then the student and I will try to request the professor of other class to accommodate us.**

Please note that EE457 exams are long (2H 50 minutes or 3 hours long) as they are design exams. I do not want to hurry you up. The three exams make up a total of about 60% of the course grade.

*One quiz (~10%), one midterm (~20%), and the final exam (~30%)*

The “Quiz” slot (Qz 5:30-8:20PM)  
We will utilize this slot only twice in the whole semester to conduct a quiz and a midterm exam. So it is OK to have schedule conflict with the quiz slot provided you agree to make yourself available for these two occasions.

**Quiz (~10%): Thursday Sep. 22, 2016 05:30 PM - 08:20 PM PST**  
**Midterm (~20%): Thursday Oct. 27, 2016 05:30 PM - 08:20 PM PST**

![Nov. 11 | Last day to drop a class with a mark of “W”](http://classes.usc.edu/term-20163/calendar/)

Note: EE457 Final Exam is as per the Exceptions Schedule posted at the bottom of:  
http://classes.usc.edu/term-20163/finals/

**Final Exam (~30%): Saturday, Dec 10, 2016 01:15 AM - 04:15 PM PST** (official slot of 02 PM to 04 PM) extended by 1 hour by starting 45 minutes early and ending 15 minutes late).

d) Grading Policy:

<table>
<thead>
<tr>
<th>Course weights</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assignments</td>
<td>Late submission penalty for assignments</td>
</tr>
<tr>
<td>Homeworks</td>
<td>~7% 5% per day up to 3 days if solution is not given out</td>
</tr>
<tr>
<td>Labs</td>
<td>~ 28% 3% flat penalty up to 3 days</td>
</tr>
<tr>
<td>Class participation</td>
<td></td>
</tr>
<tr>
<td>Short exercises</td>
<td>~ 5% In-class exercises, short exercises posted on D2L, etc.</td>
</tr>
<tr>
<td>Exams</td>
<td></td>
</tr>
<tr>
<td>Quiz</td>
<td>~ 10% no make-up exam</td>
</tr>
<tr>
<td>Midterm</td>
<td>~ 20% no make-up exam</td>
</tr>
<tr>
<td>Final</td>
<td>~ 30% no make-up exam</td>
</tr>
</tbody>
</table>

**Penalty** for lecture absence: 1% of the course for the 3rd and the 4th; 2% for the 5th and there after  
**Penalty** for discussion absence: 0.5% for the 3rd and the 4th; 1% for the 5th and there after
e) Academic Accommodations:

Any student, requiring academic accommodations based on a disability, is required to register with the Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester. A letter of verification for approved accommodations can be obtained from CAS & DSP. Please make sure that the letter is delivered to me as early in the semester as possible (no less than 2 weeks before an exam). The CAS & DSP office is located in STU 301. Their phone number is (213) 740-0776.

http://sait.usc.edu/academicsupport/centerprograms/dsp/home_index.html

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind. If you miss more than 5 lecture meetings, you may as well drop the course. It is a design course requiring continuity in your learning process. So please attend every lecture meeting. The following penalty rules do not apply to remote students, as I cannot monitor their attendance. They are allowed to watch the lecture in the evening/late night.

Penalty for lecture absence: 1% for the 3\textsuperscript{rd} and the 4\textsuperscript{th}; 2% for the 5\textsuperscript{th} and after.
Penalty for discussion absence: 0.5% for the 3\textsuperscript{rd} and the 4\textsuperscript{th}; 1% for the 5\textsuperscript{th} and after.

http://www-classes.usc.edu/engr/ee-s/457/EE457_attendance_policy.html

Homeworks shall be done individually. In-class exercises or short exercises posted on D2L (covering about 5% of the course grade) can be done taking help from fellow students but each student shall submit individually his/her completed work. Design and simulation labs can be performed either individually or in teams of two students (2 per team). But occasionally, design labs may be assigned as individual assignments.

Teams shall submit one set of Verilog code and results online. However justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment (paper submissions), shall be prepared individually. Copying is different from discussing ideas with other students.

You are encouraged to share your thoughts on homework, design labs, and design lab reports with others as long as you act like a Teaching Assistant who tries to help without giving away the solution. Absolutely no copying. Do NOT try to copy any assignment. We have ways to find if a design/simulation lab has been copied. Try not submitting a non-working lab as we give very little credit for a non-working lab.

We are here to help you and guide you in your debugging. If you submit a non-working design/lab and if do not write on the top of it in BIG letters that it is NOT WORKING (and further do not inform the instructor, the TAs, and the lab graders through an email before submission), we will treat it as an attempt to cheat. This is very important.

Academic dishonesty cases will be dealt with severely. You must have gone through the short tutorial on Academic Integrity at USC posted at

https://libraries.usc.edu/research/reference-tutorials

Try to see which version works for you (one with _html5 and the other without)
http://lib-php.usc.edu/libraries/about/reference/tutorials/avoiding-plagiarism/story.html
http://lib-php.usc.edu/libraries/about/reference/tutorials/avoiding-plagiarism/story_html5.html

Another important resource is the Student Judicial Affairs and Community Standards (SJACS) website. You may also want to visit

https://studentaffairs.usc.edu/scampus/
University policy requires that all academic integrity violations are reported to Student Judicial Affairs and Community Standards (SJACS).

We will try to make the assignments due on times far from the class time. This is to make sure that students do not miss classes to complete their assignments.

Please check your email regularly. Also visit the DEN D2L regularly at https://courses.uscden.net/ D2L stands for Desire2Learn, a Learning Management System used by DEN. https://gapp.usc.edu/graduate-programs/den/technical-support/Desire2Learn

4. Design/simulation labs sequence:

Example Weights of the labs: Note that some labs have zero weights as you are not asked to submit these labs. However you are still responsible for reading the lab design and are able to answer questions on these items also on the exams. Labs and HWs vary slightly from semester to semester. The list below is from a recent semester.

<table>
<thead>
<tr>
<th>RTL LABS</th>
<th>CPU LABS</th>
</tr>
</thead>
<tbody>
<tr>
<td>#</td>
<td>Points</td>
</tr>
<tr>
<td>1P1</td>
<td>100</td>
</tr>
<tr>
<td>1P2</td>
<td>100</td>
</tr>
<tr>
<td>1P3_M1</td>
<td>100</td>
</tr>
<tr>
<td>1P3_M2</td>
<td>100</td>
</tr>
<tr>
<td>1_paper</td>
<td>100</td>
</tr>
<tr>
<td>2_Merge_P2</td>
<td>100</td>
</tr>
<tr>
<td>2_Merge_P4</td>
<td>100</td>
</tr>
<tr>
<td>2_Merge_Paper</td>
<td>115</td>
</tr>
<tr>
<td>FIFO_P1</td>
<td>100</td>
</tr>
<tr>
<td>FIFO_P2</td>
<td>100</td>
</tr>
<tr>
<td>3_paper</td>
<td>100</td>
</tr>
<tr>
<td>3</td>
<td>100</td>
</tr>
<tr>
<td>ROB_P2</td>
<td>100</td>
</tr>
</tbody>
</table>

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week.

The labs make up 25% to 30% of your course credit.

0) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1, Part #2, Part #3 (M1, M2, M3, M4)

2) Merge Sort lab Lab#2 Part #2 and Part #4

3) Design of a 32-bit ALU Lab #3
4) FIFO and its application

5) Multi-cycle CPU Design Lab #4 Part #4 (only paper submission)

6) Pipeline labs
   Design of a 3-element adder Lab #7 Part #1, #2,
   Design of a simple pipeline Lab 7 Part #3 (Sub parts SP1, SP2)
   RTL Coding of a simple pipeline Lab 7 Part #3 (Sub parts SP3, SP3)

7) Design of a Pipelined CPU Lab #6 Part #4 and Part #5 (only paper submission)

8) ROB and its application

5. Readings:

The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself. Students, who postpone reading, gradually drift away from the rest of the class and eventually perform very poorly on the exams and design/simulation labs.

Primary References:

Class Notes (required): Please buy from the university (USC) bookstore. Remote students can place their orders online for the class notes and other items at the following (They may have to wait for a week to place their order):
USC Bookstores => Book Division => Distance Education
http://uscbookstore.com/courselistbuilder.aspx
If there is any problem, please call (213) 740-TEXT and also let me know if the problem cannot be resolved.

Lab Manual: We prefer to distribute the lab assignments progressively as pdf files. We can review and revise each assignment (if needed) and post it on the D2L.

Textbook/Verilog Guide:
   By D. A. Patterson (Berkeley) and J. L. Hennessey (Stanford)
   We do not use the textbook that much. Some students manage without the textbook. But this is a very good book to buy and keep.
   You can buy it from the university (USC) bookstore or any place (such as online bookstores).
   If you have the 4th edition, that is fine too.

2. The Verilog 2001 Reference Guide by Esperan (Cadence)
   You need this for your Verilog-based design/simulation labs. You can use it in the EE457 exams.
   Esperan (Cadence) does not sell it to individuals. They provided the pdf file to us free. It is posted on the D2L. We will bring a few printed copies to the exam hall and you can borrow a copy for a short time.

Secondary References (Do not buy these):
2. EE557 Textbook: Parallel Computer Organization and Design by Dubois, Annavaram, and Stenstrom
6. **Course Schedule** by week for Fall 2016:

Chapter numbers point to chapters in my class notes [here](http://www.ices.usc.edu/~baha/EE457/EE457_Classnotes/).

Homeworks and labs due dates are posted in a calendar and you will be provided with a link to the same.

<table>
<thead>
<tr>
<th># of lectures</th>
<th>Lecture #</th>
<th>Item</th>
<th>Homework /Lab</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1, 2 Week #1 8/22-8/25</td>
<td>Ch#1 Intro to course, review of prerequisite material, Review data path and control unit design, Moore and Mealy, Glitches in control signals, Data registers with Data enable, State diagram design, All Inclusive and Mutually Exclusive rules,</td>
<td>HW#1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Verilog coding: Watch the 6-part EE354L lectures at home and learn by yourself. Install Modelsim and learn to use the tool by yourself.</td>
<td>Tools installation</td>
</tr>
<tr>
<td>1</td>
<td>3 Week #2 8/29-8/30</td>
<td>Compare and contrast: state diagram vs. flow-chart, Min-Max (a 6-part lab)</td>
<td>Lab #1</td>
</tr>
<tr>
<td>1</td>
<td>4 Week #2 8/31-9/1</td>
<td>Ch#2 Performance, MIPs, MFLOPs</td>
<td>HW #2</td>
</tr>
<tr>
<td>2</td>
<td>5, 6 Week #3 9/5-9/8</td>
<td>Ch#3 MIPs ISA, SLT, SLTU lw, sw, Byte addressable processors, memory addresses, also cover word addresses in a byte addressable processor</td>
<td>HW#1B</td>
</tr>
<tr>
<td>2</td>
<td>7, 8 Week #4 9/12-9/15</td>
<td>Ch#4 P1 Review overflow detection in unsigned and signed arithmetic and ALU design</td>
<td>ALU lab Lab #3</td>
</tr>
<tr>
<td>2</td>
<td>9, 10 Week #5 9/19-9/22</td>
<td>Ch#5 P1 Single Cycle CPU,</td>
<td>HW #5A (Single-cycle CPU)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Quiz exam on Thursday Sept. 22, 2016 5:30PM-8:20PM in ------</td>
<td>Quiz slot</td>
</tr>
<tr>
<td>Week</td>
<td>Topics</td>
<td></td>
<td></td>
</tr>
<tr>
<td>------</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
| 11, 12 | Week #6 9/26-9/29  
Ch#5 P2 multi-cycle CPU Datapath and control design  
Ch#5 P2 Multi-cycle CPU 2nd edition design |
| 13, 14, 15, 16 | Week #7, 8 10/3-10/13  
Ch#6 5-stage pipeline: data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. Also cover exceptions. |
| 17, 18 | Week #9 10/17-10/20  
Ch#7 P1 Cache: Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs, |
| 19, 20 | Week #10 10/24-10/27  
Ch#7 P2 Virtual memory: Multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory |
| 21, 22 | Week #12 10/31-11/3  
Virtual memory, Exceptions, Branch Prediction, 1-bit and 2-bit predictors, BPB, BTB |
| 23, 24 | Week #13 11/7-11/10  
Out of order execution and Tomasulo Part 1 (lol,OoE,OoC), WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, RST, issue queues, issue unit, CDB, |
| 25, 26 | Week #14 11/14-11/17  
Tomasulo Part 2 (lol,OoE,loC), ROB, ROB search, Speculative execution beyond predicted branches, and selective flushing if branch was mispredicted, exception handling, |
Ch#8 Parallel processing, semaphores, Read-Modify-Write (RMW) race, atomic operations on shared variables, CMP, Snoopy Cache Coherency protocols, Write through vs. write-back, MSI, MOESI |
| 29, 30 | Week #16 11/30-12/1  
CMT, Thread-level parallelism, MPI, non-blocking cache, Locks, Mutual Exclusion, LL and SC instructions in MIPs |
| 30 | Week #17  
Ch#4 P2 CLA (Carry Look-ahead Adder) |

**Midterm exam on Thursday October 27, 2016 5:30PM-8:20PM in ------**

**Thanksgiving Recess Nov 23-26**

**Classes end on Dec. 2, 2016 Friday. Study Days Dec 5-7**

**Final exam on Saturday Dec 10, 2016 1:15PM – 4:15PM**

See the exceptions list at the bottom of [http://classes.usc.edu/term-20163/finals/Electrical Engineering 109, 209, 457](http://classes.usc.edu/term-20163/finals/Electrical Engineering 109, 209, 457)

Final Exam is comprehensive but focuses on later topics.
**Statement on Academic Conduct and Support Systems**

**Academic Conduct**
Plagiarism – presenting someone else’s ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Section 11, *Behavior Violating University Standards* https://scampus.usc.edu/1100-behavior-violating-university-standards-and-appropriate-sanctions/. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct/.

Discrimination, sexual assault, and harassment are not tolerated by the university. You are encouraged to report any incidents to the *Office of Equity and Diversity* http://equity.usc.edu/ or to the *Department of Public Safety* http://dps.usc.edu/. This is important for the safety of the whole USC community. Another member of the university community – such as a friend, classmate, advisor, or faculty member – can help initiate the report, or can initiate the report on behalf of another person. The *Relationship and Sexual Violence Prevention and Services (RSVP)* https://engemannshc.usc.edu/rsvp/ provides confidential support.

**Support Systems**
A number of USC’s schools provide support for students who need help with scholarly writing. Check with your advisor or program staff to find out more. Students whose primary language is not English should check with the *American Language Institute* http://ali.usc.edu/, which sponsors courses and workshops specifically for international graduate students. The *Office of Disability Services and Programs* http://dsp.usc.edu/ provides certification for students with disabilities and helps arrange the relevant accommodations. If an officially declared emergency makes travel to campus infeasible, *USC Emergency Information* http://emergency.usc.edu/ will provide safety and other updates, including ways in which instruction will be continued by means of blackboard, teleconferencing, and other technology.