Topic 4

Clocking
data registers

\( \text{Reg X} \)

\( x_{-load} \)
Common misconception

3 problems
problem # 1

clk

S₃

S₄

S₅

S₆

x-load

x≤y+2
Simple Solution:

x-load

X-reg
Problem #2

x-load can easily contain glitches
Glitches in Combinational Logic

Static-1 Hazard

Static-∅ Hazard
Problem #3

x_load
Two Solutions

a) Muxed FFs (data registers with data enable)

b) Gated Clocking (Good for low-power designs)
Muxed FFs
(data registers with data enable)
if \( x_{-\text{load}} = 1 \) Then

\[ X \leftarrow \text{Data}; \]

else

\[ X \leftarrow X; \]

end if;
Muxed FFs:
Disadvantages

1. Power ↑
2. Area ↑
3. not suitable for latches, RAMs, asynchronous operations

Solution: Gated clocking
The only way to STOP updating or changing the contents of 74LS175 is by INHIBITING its CLOCK using a gate (generally known as GATED CLOCKING). This is NOT DESIRABLE because of CLOCK SKEW and GLITCHES.

SN74LS173A
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

logic diagram

CLOCK need not be inhibited to STOP loading. Disable its data inputs, then it's register loads its current content back into itself.
74LS163A SYNCHRONOUS 4-BIT COUNTER

Pin numbers shown on logic notation are for D, J or N packages.
74LS163A
Synchronous 4-bit counter with enable control

Synchronous 4-bit counter
Synchronous clear
Synchronous load
Enable Controls ENP, ENT
Clock is never inhibited; when disabled the D-FFs load their current contents back into themselves.
What is a DATA REGISTER?

What is a CONTROL REGISTER?