The pseudo code for the Early Branch design:

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**FU (the original Forwarding Unit in EX stage):**

1. **EX Hazard:**

   if [ 
   
   | EX/MEM.RegWrite 
   | and (EX/MEM.WriteRegister /= 0) 
   | and (EX/MEM.WriteRegister == ID/EX.ReadRegister_RS) 
   ]
   
   then make FW_RS_MEM = 1 (i.e. make ALUSelA = 10; make EX1 = true)

   if [ 
   
   | EX/MEM.RegWrite 
   | and (EX/MEM.WriteRegister /= 0) 
   | and (EX/MEM.WriteRegister == ID/EX.ReadRegister_RT) 
   ]
   
   then make FW_RT_MEM = 1 (i.e. make ALUSelB = 10; make EX2 = true)

2. **MEM Hazard:**

   if [ 
   
   | MEM/WB.RegWrite 
   | and (MEM/WB.WriteRegister /= 0) 
   | and (MEM/WB.WriteRegister == ID/EX.ReadRegister_RS) 
   | and (EX1 /= true) 
   ]
   
   then make FW_RS_WB = 1 (i.e. make ALUSelA = 01)

   if [ 
   
   | MEM/WB.RegWrite 
   | and (MEM/WB.WriteRegister /= 0) 
   | and (MEM/WB.WriteRegister == ID/EX.ReadRegister_RT) 
   | and (EX2 /= true) 
   ]
   
   then make FW_RT_WB = 1 (i.e. make ALUSelB = 01)

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FU_Br (New Forwarding Unit in ID stage to serve the early branch):

If [ 
    EX/MEM.RegWrite 
    and (EX/MEM.WriteRegister /= 0) 
    and (EX/MEM.WriteRegister == IF/ID.ReadRegister_RS) 
] 
then make FW_RS = 1

If [ 
    EX/MEM.RegWrite 
    and (EX/MEM.WriteRegister /= 0) 
    and (EX/MEM.WriteRegister == IF/ID.ReadRegister_RT) 
] 
then make FW_RT = 1

HDU (Original Hazard Detection Unit in ID stage):
Note: Here ID/EX.WriteRegister refers to the WriteRegister after the mux governed by RegDst.
We could replace it with ID/EX.WriteRegisterRt.

If [ 
    ID/EX.MemRead 
    and (ID/EX.WriteRegister /= 0) 
    and 
    {
        (ID/EX.WriteRegister == IF/ID.ReadRegister_RS) 
        or 
        (ID/EX.WriteRegister == IF/ID.ReadRegister_RT)
    } 
] 
then make STALL_LW = 1

HDU_Br (New Hazard Detection Unit in ID stage to serve the early branch):
Note: Here ID/EX.WriteRegister refers to the WriteRegister after the mux governed by RegDst.

If [ 
    Branch 
    and [ 
        [ 
            ID/EX.RegWrite 
            and (ID/EX.WriteRegister /= 0) 
            and 
            {
                (ID/EX.WriteRegister == IF/ID.ReadRegister_RS) 
                or 
                (ID/EX.WriteRegister == IF/ID.ReadRegister_RT)
            } 
        ] 
        or 
        [ 
            EX/MEM.MemRead 
            and (EX/MEM.WriteRegister /= 0) 
            and 
            {
                (EX/MEM.WriteRegister == IF/ID.ReadRegister_RS) 
                or 
                (EX/MEM.WriteRegister == IF/ID.ReadRegister_RT)
            } 
        ] 
    ] 
] 
then make STALL_BEQ = 1