Study Questions

EE 477 University of Southern California

1. In an inverter, what regions of operation are the transistors in when the short circuit current is maximum?

2. The graph below shows the output of an inverter when the input changes from 0 to 5 V. and 5 V. to 0. What is the average delay of the inverter? What is the rise time? What is the fall time?

3. The equation below describes some properties of the circuit shown. What quantity does each side of the equation represent? What circuit law allows us to equate these two expressions?

\[
\frac{C_{out}dV_{out}}{dt} = \beta \left[ V_{ds}(V_{gs}-V_{thn}) - \frac{V_{ds}^2}{2} \right]
\]

4. An inverter chain has three inverters. The first one has minimum size transistors. The second has transistors 3 times wider than minimum, and the third has transistors 9 times wider than minimum. If the first inverter alone can drive a minimum load with the required delay, how big a load can the inverter chain drive (as a function of minimum load)? Why did the designer pick 3 for the inverter size increase?

5. Compute as accurately as you can the rise time for an inverter. Assume \( C_L = 1 \) pf. and \( \beta_p = 31.9 \mu a/V^2 \) for a minimum size transistor, and the PMOS transistor in the inverter is minimum width but two times minimum length. Assume \( V_{dd} = 5 \) V. and \( V_{thp} = -1 \) V.
6. Show the equivalent circuit of the transistor circuit shown below at the instant when $V_{in}$ rises to 5 V, assuming $A = 5$ V and $V_{out}$ initially is 5V. Include all the capacitances and resistances you can, including the interconnect.