1. The given boolean expression is:

\[ A = D_1(D_2 + D_3) + (/D_1 + /D_2)(D_4) \]

(a) We can re-arrange the above equation so that we can find an Euler’s path:

The rearranged equation is:

\[ A = D_1(D_2 + D_3) + D_4(/D_1 + /D_2) \]
The Euler’s path for the above circuit is:
D3-D2-D1-D4-/D2-/D1

This is just one of the possible Euler paths.

(b) **Stick diagram:**

**Color code:**

Red: Polysilicon

Green: N-diffusion

Brown: P-diffusion

Purple – M2

Blue – M1
2. Layout of the inverter:
3. **Accumulation** is the term used to describe the state of the channel when $V_{gs}<0$, for an NMOS transistor. In this state, there is no channel formed, and the only charges that exist under the gate are the mobile holes of the P-doped substrate. As such, these will not result in conduction, and are not useful charges as far as the NMOS transistor operation is concerned.

4. Poly has to extend beyond the diffusion when they cross, to safeguard against the inadvertent shorting of the source and diffusion regions during fabrication. This is known as **gate extension**.