1. Given:

\( V_{in} = 1V, \quad V_{tp} = -1V \).

\( \frac{R_m}{R_p} = 1.5 \) \& \( V_{DD} = 5V \).

We have:

\[
V_{in} = \frac{V_{DD} + V_{tp} + V_{in}}{1 + \sqrt{\frac{R_m}{R_p}}}
\]

\[
V_{in} = \frac{5 + (-1) + 1(\sqrt{1.5})}{1 + \sqrt{1.5}}
\]

\[ V_{in} = 2.349V \]

2. For PIN diode transistor:

Given:

\( V_{gs} = -2.5V, \quad V_{tp} = -1V \).

For PIN diode transistor to be in saturation:

\( V_{DS} < V_{gs} - V_{tp} \).

\[ V_{DS} < -2.5 - (-1) \]

\[ V_{DS} < -1.5 \]
$V_{DS}$ can have any value less than $-1.5V$.

3) For NMOS transistor

\begin{align*}
V_{AS} &= 2.5V \\
V_{GS} &= 1.4V \\
V_{TN} &= 1V
\end{align*}

Since $V_{DS} < V_{AS} - V_{TN}$ the NMOS transistor is in linear region.

When $V_{GS} = 1.5V$ and $V_{DS} = 2.6V$

Since $V_{DS} > V_{GS} - V_{TN}$ the NMOS transistor is in saturation region.

4) Rise in threshold voltage of NMOS transistor in due to the fact that its source voltage is not zero (0) tied to ground. (01) due to body effect.

We know

$$I_{DS} \propto (V_{GS} - V_{TN})$$

From above equation we see that as $V_{TN}$ increases current $I_{DS}$ decreases for same $V_{GS}$ and $V_{DS}$ voltage values.
Transistors 2, 4, 5, 6, 7, 9, 11 will be subjected to body effect.

At

\[ V_{in} = 5V \]
\[ V_{out} = 0V \]

Given: \( t = 0 \) \( S \) rises from 0 to 5V instantly

Considering \( P \) heats transistor \( C \)

\[ V_{in} = 5V \]
\[ V_{out} = 0V \]
At $t=0^+$

$$V_{GSS} = V_G - V_S = 0.5 - 5 = -5V.$$  

$$V_{DSS} = V_D - V_S = 6.5 - 5 = 1.5V.$$  

As $V_{GSS} < V_{TP}$ and $V_{DSS} < V_{GSS} - V_{TP}$.

The PMOS transistor is in a saturation.

As time $t$ is elapsed, the voltage of Drain increases and at $t=\infty$ $V_{out} = V_D = 5V$.

Then $V_{DSS} > V_{GSS} - V_{TP}$ & $V_{GSS} < V_{TP}$.

PMOS transistor is in a linear region.

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$$V_{GSS} = 0.5V$$

$$V_{DSS} = 1.5V$$

$$V_{out} = 5V$$

$$V_{GSS} = V_G - V_S = 0.5 - 5 = -5V.$$  

$$V_{DSS} = V_D - V_S = 6.5 - 5 = 1.5V$$

$V_{GSS} < V_{TP}$ & $V_{DSS} > V_{GSS} - V_{TP} - 0.5V$.

Hence in saturation region.
As parasitic capacitors discharge & when the voltage across it drops to 4.5V.

\[ V_{DS} = 0V \]

Then, hence there will be no path for capacitor to discharge & therefore the final value of \( V_{DS} \) is 4.5V.

\[ \begin{align*}
V_{in} &= 4.5V \\
V_{out} &= 5V \\
V_{DS} &= 4.5V
\end{align*} \]

\[ V_{GS} = V_{G} - V_{S} = 0.5V \]

\[ V_{GS} > V_{th} \]

The transistor is in cutoff & final value of \( V_{DS} = 5V \).

Noise margin = \( N_{HL} = V_{in} - V_{th} \)

\[ N_{HL} = 1.7 - 1.6 = 0.1V \]

The inverter will have a noise problem if noise amplitude is greater than 0.1V.

If noise amplitude is \( < 0.05V \) there will be no noise problem.

If noise amplitude is \( < 0.8V \) there will be no problem due to noise.