At t=\infty,

The output voltage $V_{\text{out}}$ is 2V because the PMOS transistor is ON. Therefore, the NMOS transistor is in cutoff because $V_{\text{gsn}}=0V$, which is less than $V_{\text{tnbodyeffect}}$.

Assuming the PMOS transistor is in linear region:

\[
V_{\text{dsp}} > V_{\text{gsp}} - V_{\text{tnbodyeffect}} \\
2-2 > 0-2 -\text{(-.9)} \\
0 > 2+.9 \\
0 > 1.1
\]

The assumption is true; therefore the PMOS transistor is in LINEAR region.
2) To remain in segment A, we need that the PMOS stays in linear region and the NMOS in cutoff. Therefore, the minimum \( V_{out} = V_{DD} \).

3) To remain in the D segment, we need that the PMOS stays in saturation and the NMOS in linear region.

So,

\[
OV < V_{out} < \frac{V_{DD}}{2} - V_{thn}
\]

4) \( R_{chp} = \frac{1}{P_{p} \left( V_{gsP} - V_{thp} \text{ body effect} \right)} \)

\[
= \left| \frac{1}{(51 \times 10^{-6})(\frac{4}{2}) \left( -1.1 - (-.9) \right)} \right|
\]

\( = 49 \text{ k}\Omega \)
5) In segment D, the NMOS is in linear region, and the PMOS is in saturation region. Thus,

\[ V_{ds} < V_{gs} - V_{th} \]
\[ V_{out} - V_{dd} < V_{in} - V_{dd} - V_{th} \]
\[ V_{out} < 1.6 + .7 \]
\[ V_{out} < 2.3 \]

NMOS:
\[ V_{ds} = V_{gs} - V_{th} \]
\[ V_{out} = V_{in} - V_{th} \]
\[ V_{out} < 1.6 - .7 \]
\[ V_{out} < .9 \text{V} \]

The output voltage that satisfies both conditions is
\[ V_{out} = .9 \text{V} \]

6) In segment C, both transistors are in saturation. If the \( E \)'s are equal, then the input voltage \( V_{in} = \frac{V_{dd}}{2} \).

\[ V_{out} \text{ vs. } V_{in} \]

Looking at the input-output characteristic (\( I_{out} \text{ vs. } V_{in} \)),
when the input voltage is \( \frac{V_{dd}}{2} - E \), where \( E \) is a small value
the PMOS is in linear region and NMOS is in saturation region. If the
input voltage \( V_{in} \) keeps increasing, then at some point (segment C) the
pmos moves to saturation region. When the input is greater than
\( \frac{V_{dd}}{2} \), the NMOS transistor moves to linear region thus the output current
decreases. So, in segment C, the output current reaches its max value.
If the C segment occurs when $V_{in} = V_{dd}/2$ it tells us that $P_p > P_n$.

7) $V_{in} = 1.2$, which is greater than $V_{th0}$, the NMOS is ON and the pMOS is OFF. Since $P_p / P_n = 2$, it implies that the C segment occurs at a voltage greater than $V_{DD}/2$. Therefore, because $V_{in} = 1.2$ is less than $1.25V$ the inverter is in Segment B, where the NMOS is in saturation and the PMOS is in linear region.

8) The spacing is to avoid shorts between the p+ diffusion and the p-substrate.

9) Yes, there is net charge, which is negative. This is because before applying a positive gate voltage, the p-sub is neutral, consisting of negative fixed charge and positive movable charge (hole). After the application of positive gate voltage, the holes are pushed off to bottom (this is an equivalent phenomenon of that the electrons are pulled up to neutralize the holes near the channel), leaving negative charges in the depletion region.