Problem 1

a) Equal PMOS and NMOS betas will give rise and fall times that are about equal. Equal betas allow for good safety noise margins, and the high and low noise margins are equal. Also, the crossover point on the inverter input/output transfer curve will occur at $V_{in} = V_{dd}/2$.

b) Larger chips are more expensive than smaller chips because they require more materials during fabrication and processing. Larger chips require more wafers since they take up larger areas. More chemicals and metals are needed to create the different layers. Also, it may cost more to operate equipment if more wafers need to be used. The main reason for larger chips being more expensive is that the odds of a defect causing failure are higher. And hence more chips have to be fabricated to get an equal number of working dies.

Problem 2

In segment B, the NMOS is in saturation and the PMOS is in the linear region.

For the NMOS to be in saturation,

\[ V_{dsn} > V_{gsn} - V_{tn} \]
\[ V_{out} > V_{in} - V_{tn} \]
\[ V_{out} > 0.8 - 0.7 \]
\[ V_{out} > 0.1V \]

For the PMOS to be in the linear region,

\[ V_{dsp} > V_{gsn} - V_{tp} \]
\[ V_{out} - V_{dd} > V_{in} - V_{dd} - V_{tp} \]
\[ V_{out} > 0.8 - (-0.7) \]
\[ V_{out} > 1.5 \]

Based on these conditions, the minimum value that would allow the inverter to stay in segment B is $V_{out} = 1.5V$.

Problem 3

Show that the PMOS is in cutoff:

\[ V_{gsn} > V_{tp} ? \]
\[ V_{in} - V_{dd} > V_{tp} ? \]
\[ 1.2 - 1.8 > -0.7 ? \]
Thus the PMOS is in cutoff.

In segment E, the NMOS is in the linear region.

\[ V_{dsn} < V_{gsn} - V_{tn} \]
\[ V_{out} < V_{gsn} - V_{tn} \]
\[ V_{out} < 1.2 - 0.7 \]
\[ V_{out} < 0.5 \]

The maximum voltage to stay in segment E is \( V_{out} = 0.5V \).

**Problem 4**

The drain of the transistor is at the input, and the source is at the output. To pass a “1”, the input is \( V_{in} = V_d = V_{dd} \). In order for the NMOS transistor to stay ON, \( V_{gsn} \geq V_{tn} \). This means that the maximum value that the source/output can charge up to is \( V_s = V_{out} = V_g - V_{in} = V_{dd} - V_{in} \), if the gate voltage is \( V_{dd} \).

So, the output can never pass the full value of \( V_{dd} \), and the NMOS can only pass weak “1’s”. In fact, due to body effect, the output voltage is even weaker than expected, \( V_{dd} - V_{in} \).

**Problem 5**

a) \( \beta_{ppn} = V_{gsn} - V_{tn}^2 \frac{V_{dsn} - V_{dd} - V_{tp2}}{V_{gsn} - V_{dsn} - V_{tn}^2} = 0.85 - 0.7 + 2(0.85 - 0.7)2 = 0.36 \)

b) The NMOS is unit size, so \( W = 4\lambda, \ L = 2\lambda \).

\( \beta_n = 219.442 = 438.8 \ \mu A/V^2 \)
\( \beta_{ppn} = \beta_p 438.8 = 0.36 \)
\( \beta_p = 157.96 \ \mu A/V^2 \)

Assume the PMOS transistor has minimum length \( L_p = 2\lambda \).

\( \beta_p = 51W_p2\lambda = 157.96 \ \mu A/V^2 \)
\( W_p = 6.19\lambda \)

The dimensions of the PMOS transistor are \( L_p = 2\lambda, \ W_p = 6\lambda \)

**Problem 6**

The minimum \( V_{in} \) for the inverter to be in segment D occurs at the crossover point in segment C. The crossover point can be found with:

\[ \beta_{ppn} = V_{gsn} - V_{tn}^2 \frac{V_{dsn} - V_{dd} - V_{tp2}}{V_{gsn} - V_{dsn} - V_{tn}^2} \]
\[ 2 = V_{gsn} - 0.72 V_{gsn} - 1.8 + 0.72 = V_{gsn}^2 - 1.4V_{gsn} + 0.49V_{gsn}^2 - 2.2V_{gsn} + 1.21 \]
\[ V_{gsn2} - 3V_{gsn} + 1.93 = 0 \]
\[ V_{gsn} = 3 \pm 32 - 411.932 \]
\[ V_{gsn} = 2.066V, 0.935V \]
Both transistors are in saturation at segment C. This requires that:
\[ V_{dsn} > V_{gsn} - V_{tn} \]
\[ V_{dd2} > V_{gsn} - V_{tn} \]
\[ 0.9 > V_{gsn} - 0.7 \]
\[ V_{gsn} < 1.6V \]
The only value that satisfies this is \( V_{gsn} = 0.935V \). This is the crossover point at segment C.
For the inverter to be in segment D, the input should be greater than the crossover point at segment C. Thus, the minimum value that will allow the inverter to stay in segment D is \( V_{in} = 0.935V \).

**Problem 7**
Poly gate extension is used to prevent leakage current between the source and drain. Without gate extension, impurities may scatter outside the gate area during the diffusion process when the source and drain are created. Current may leak between source and drain even when the gate is OFF if there are enough impurities outside the channel.

**Problem 8**
Both the gate-source and drain-source voltages control current flow in the channel. In saturation, the voltage at the drain is equal to or lower than the voltage at the gate shifted by the threshold voltage. The pn-junction at the drain/n-well interface is reverse-biased due to the lower potential at the drain. The reverse bias starts to deplete charges from the area surrounding the drain. This decreases the channel on the drain-side.