Problem 1

a) Worst-case fall time path: E = F = A = 1, B = C = D = G = 0

Lumped model delay:

\[ RC_{\text{fall}} = 4 R_{\text{chn}} (13C_{\text{dn}} + 10C_{\text{dp}}) \]

b) Elmore delay:

\[ RC_{\text{fall}} = R_{\text{chn}} (13C_{\text{dn}} + 10C_{\text{dp}}) + R_{\text{chn}} (8C_{\text{dn}} + 10C_{\text{dp}}) + R_{\text{chn}} (4C_{\text{dn}} + 10C_{\text{dp}}) + R_{\text{chn}} (2C_{\text{dn}} + 10C_{\text{dp}}) = R_{\text{chn}} (27C_{\text{dn}} + 40C_{\text{dp}}) \]
Problem 2

a) Long wires using π-model

Rise Time Equivalent Circuit:

\[ RC_{\text{rise}} = R_{\text{chp}}(16C_{\text{dn}} + 2C_w) + R_{\text{chp}}(14C_{\text{dn}} + 2C_w) + R_{\text{chp}}(12C_{\text{dn}} + 2C_w) + R_w\left(6C_{\text{dn}} + \frac{C_w}{2}\right) = R_{\text{chp}}(42C_{\text{dn}} + 6C_w) + R_w\left(6C_{\text{dn}} + \frac{C_w}{2}\right) \]

\[ = 4000(42 \times 10 + 6 \times 6)(10^{-15}) + 10\left(6 \times 10 + \frac{6}{2}\right)(10^{-15}) \]

\[ RC_{\text{rise}} = 1.825 \text{ ns} \]

Fall Time Equivalent Circuit:
\[ RC_{fall} = R_{chn}(16C_{dn} + 2C_w) + R_w \left( 6C_{dn} + \frac{C_w}{2} \right) \]
\[ = 1000(16 \times 10 + 2 \times 6)(10^{-15}) + 10 \left( 6 \times 10 + \frac{6}{2} \right)(10^{-15}) \]

\[ RC_{fall} = 173 \text{ ps} \]

The rise time at the input of the transmission gate is much larger than the fall time. It is about 10 times larger than the fall time.

b) Insert inverters 1/3 and 2/3 of the way along the long wires. Find fall time constants.

Since the wire lengths are decreased to L/3, the wire resistances and capacitances are decreased to \( R_w/3 \) and \( (1/3)(C_w/2) = C_w/6 \).

Fall Time Equivalent Circuit at Input of 1st Inverter:
Since \( C_{dp} = C_{dn} = C_{gp} = C_{gn} \),

\[
R_C_{fall} = R_{chn} \left( 12C_{dn} + \frac{2}{3}C_w \right) + R_w \left( C_{gp} + C_{gn} + \frac{C_w}{6} \right) \\
= R_{chn} \left( 12C_{dn} + \frac{2}{3}C_w \right) + \frac{R_w}{3} \left( 2C_{dn} + \frac{C_w}{6} \right) \\
= 1000 \left( 12 \times 10 + \frac{2}{3} \times 6 \right) (10^{-15}) + \frac{10}{3} \left( 2 \times 10 + \frac{6}{6} \right) (10^{-15}) = 124 \text{ ps}
\]

Rise Time Equivalent Circuit at Input of 2\textsuperscript{nd} Inverter:

\[
R_C_{rise} = R_{chp} \left( 4C_{dn} + \frac{C_w}{3} \right) + \frac{R_w}{3} \left( 2C_{dn} + \frac{C_w}{6} \right) \\
= 4000 \left( 4 \times 10 + \frac{6}{3} \right) (10^{-15}) + \frac{10}{3} \left( 2 \times 10 + \frac{6}{6} \right) (10^{-15}) = 168 \text{ ps}
\]

Fall Time Equivalent Circuit at Input of Transmission Gate:

\[
R_C_{fall} = R_{chn} \left( 8C_{dn} + \frac{C_w}{3} \right) + \frac{R_w}{3} \left( 6C_{dn} + \frac{C_w}{6} \right) \\
= 1000 \left( 8 \times 10 + \frac{6}{3} \right) (10^{-15}) + \frac{10}{3} \left( 6 \times 10 + \frac{6}{6} \right) (10^{-15}) = 82 \text{ ps}
\]

Fall Time Constant at Input of Transmission Gate:

\[
R_C_{fall} = (124 + 168 + 82) \text{ ps} = 374 \text{ ps}
\]

Fall Time Constant at Input of 1\textsuperscript{st} Inverter:

\[
R_C_{fall} = 124 \text{ ps}
\]
The fall time delay at the input of the transmission gate is more than 2 times slower than the delay found in Part (a). So, inserting a pair of inverters along the long wires doesn’t help circuit performance. Also, the delay at the input of the first inverter is close to the delay from Part (a). So wire resistance and wire capacitance do not affect the circuit delay by much.

**Problem 3**

The clock period for a combination of flip-flops is: \( T \geq t_Q + t_{comb} + t_{setup} \).

From the flip-flop timing diagram, \( t_Q = 4.4 \, \text{ns} - 4 \, \text{ns} = 0.4 \, \text{ns} = 400 \, \text{ps} \).

From the inverter timing diagram, \( t_{comb} = 0.1 \, \text{ns} - 0 \, \text{ns} = 0.1 \, \text{ns} = 100 \, \text{ps} \).

The setup time is specified to be \( t_{setup} = 200 \, \text{ps} \).

Ignoring the propagation delay through the first latch in the flip-flop, the minimum clock period is:

\[
T = 400 \, \text{ps} + 100 \, \text{ps} + 200 \, \text{ps} = 700 \, \text{ps}
\]

**Problem 4**

\[
a(\ln a - 1) = \frac{C_d}{C_g} = 3
\]

\[
\Rightarrow a \approx 5
\]

\[
n = \frac{\ln \left( \frac{C_{load}}{C_g} \right)}{\ln a} = \frac{\ln \left( \frac{1 \, \text{pF}}{8 \, \text{fF}} \right)}{\ln 5} = 3
\]

But we need an even number of inverters. Thus, we need \( n = 4 \) stages in the inverter chain.

**Problem 5**

.......... To be added in ..........
**Problem 6**

The delay of a wire is \[ t = \frac{0.7}{2} r c l^2 \]

So the length of the wire is:

\[
l = \frac{\sqrt{2 \cdot t}}{\sqrt{0.7 \cdot r c}} = \frac{\sqrt{2 \cdot 529 \text{ ps}}}{\sqrt{0.7 \cdot (0.056 \Omega/\mu m)(50 \text{ fF/\mu m})}} = 734.7 \mu m
\]

**Problem 7**

![Diagram of a circuit with labeled components](image)

Unit size transistors \( \rightarrow R_p = 4R_n \)

Assume \( C_{dn} = C_{dp} = C_{gn} = C_{gp} \)

The delays for each gate are:

\[
RC_1 = RC_5 = R_n(5C_d + 2C_g) = R_n(7C_d) = 7R_n C_d
\]
\[
RC_2 = RC_4 = 2R_p(5C_d + 2C_g) = 2(4R_n)(7C_d) = 56R_n C_d
\]
\[
RC_3 = R_n(8C_d + 2C_g) = 10R_n C_d
\]
\[
RC_6 = 3R_p(8C_d + 2C_g) = 3(4R_n)(10C_d) = 120R_n C_d
\]

Delay through Gates 1-2-3-4:

\[
RC_1 + RC_2 + RC_3 + RC_4 = (7 + 56 + 10 + 56)R_n C_d = 129R_n C_d
\]

Delay through Gates 5-6-3-4:

\[
RC_5 + RC_6 + RC_3 + RC_4 = (7 + 120 + 10 + 56)R_n C_d = 193R_n C_d
\]

The longest delay is \( 193R_n C_d \) through Gates 5-6-3-4.
Problem 8

From the fringing fields figure in the textbook, the fringing field factor is:

\[ FF \approx 10 \]