1) The counter has unused states 0110 and 1100.

<table>
<thead>
<tr>
<th>UP</th>
<th>DOWN</th>
<th>Q3</th>
<th>Q2</th>
<th>Q1</th>
<th>Q0</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Using Karnaugh-maps we can find the input function for \( D_3 \), \( D_2 \), \( D_1 \), and \( D_0 \).

\[
D_3 = UP \cdot (Q_3 Q'_2 Q'_0 + Q'_3 Q_2 Q'_1) + DOWN \cdot (Q_3 Q_2 Q'_0 + Q'_3 Q'_2 Q'_1)
\]
\[
D_2 = UP \cdot (Q'_2 Q_1 Q'_0) + DOWN \cdot (Q'_2 Q'_1 Q'_0)
\]
\[
D_1 = UP(Q'_2 Q'_0 + Q'_2 Q'_0) + DOWN(Q'_3 Q'_1 Q'_0 + Q_2 Q'_2 Q'_0)
\]
\[
D_0 = 0
\]

Note: \( Q'_i \) is the complement of \( Q_i \).

Additional logic to include Load control signal:

Note: There is an assumption that Load signal will only load even values, so \( I_0 = 0 \); otherwise additional cumbersome logic needs to be implemented. If the odd number is uploaded the system will consider it as the smaller nearest even number.

\[
D_3 = (Load) \cdot (I_3) + (Load') \cdot [UP \cdot (Q_3 Q'_2 Q'_0 + Q'_3 Q_2 Q'_1) + DOWN \cdot (Q_3 Q_2 Q'_0 + Q'_3 Q'_2 Q'_1)]
\]
\[
D_2 = (Load) \cdot (I_3) + (Load') \cdot [UP \cdot (Q'_3 Q'_1 Q'_0) + DOWN \cdot (Q'_3 Q'_1 Q'_0)]
\]
\[
D_1 = (Load) \cdot (I_3) + (Load') \cdot [UP(Q'_2 Q'_0 + Q'_2 Q'_0) + DOWN \cdot (Q'_3 Q'_1 Q'_0 + Q_2 Q'_2 Q'_0)]
\]
\[
D_0 = I_0 \cdot 0
\]

Note, that since \( Q_0 \) is always 0, \( Q'_0 \) is 1, so we can simplify the above functions

\[
D_3 = (Load) \cdot (I_3) + (Load') \cdot [UP \cdot (Q_3 Q'_2 + Q'_3 Q'_2 Q'_1)] + DOWN \cdot (Q_3 Q_2 + Q'_3 Q'_2 Q'_1)
\]
\[
D_2 = (Load) \cdot (I_3) + (Load') \cdot [UP \cdot (Q'_3 Q'_1) + DOWN \cdot (Q'_3 Q'_1)]
\]
\[
D_1 = (Load) \cdot (I_3) + (Load') \cdot [UP(Q'_2 Q'_1 + Q'_2 Q'_1) + DOWN \cdot (Q'_3 Q'_1 + Q_2 Q'_2 Q'_1)]
\]
\[
D_0 = I_0 \cdot 0
\]
\[ D_3 = (Load) \cdot (I_3) + (Load') \cdot \left[ UP \cdot (Q_3 Q'_2 + Q'_3 Q_2 Q'_1) + DOWN \cdot (Q_3 Q_1 + Q'_3 Q'_2 Q'_1) \right] \]

\[ D_2 = (Load) \cdot (I_2) + (Load') \cdot \left[ UP \cdot (Q'_2 Q_1) + DOWN \cdot (Q'_2 Q'_1) \right] \]
\[ D_1 = (Load) \cdot (I_1) + (Load') \cdot [UP(Q'_2 Q'_1 + Q_3 Q'_2 Q_1) + DOWN \cdot (Q'_3 Q'_1 + Q_3 Q_2 Q_1)] \]

\[ D_0 = I_0 \cdot 0 \]
Positive edge-triggered D-flip flop Diagram with asynchronous reset

Another acceptable solution uses NOR gates in place of inverters

- The current output should change when the clock rises.
- Include an asynchronous reset function.
- If reset is asserted asynchronously, the current number will become 0 and should stay zero until the next positive clock edge, even if reset is subsequently unasserted.
- New data is loaded into the flip flop only when reset is not asserted. Each bit of storage should be a positive edge-triggered flip flop.
- Each flip flop should contain two latches, as described in class.
- The data loaded into the flip flop will depend on the data currently in the flip flop along with data in the other flip flops.

**Mux: first latch**

**Mux: second latch**

UP and DOWN are independent signals. When UP=1 and DOWN=0, the counter counts up, when UP=0 and DOWN=1, the counter counts down. If UP and DOWN are equal, the current circuit assumes the counter is not active. If we want to give a priority to UP or DOWN signal, then additional logic is required.
1b. (5%) Compare the flip flop designed in part 1a. with a flip flop where the multiplexers at the input to each latch are designed with NAND gates. Which one is better? Why?

The flip flop in 1a. is better since it is faster and it occupies less area. The mux implemented with transmission gates only needs 4 transistors, assuming CK and CK_bar are available, while the mux with NAND gates requires a minimum of 12 transistors. The propagation delay is smaller in the mux implemented with transmission gates.

2a. (10%) Draw a gate level implementation of the function in Problem 5 of homework 1 using only NAND gates. Assume that complement inputs are available.

\[ H = \overline{\overline{XZ(Y+W)} + \overline{P(Q+ST)U} + (N+R)(M+LOK)} \]

\[
\begin{align*}
H &= \overline{\overline{XZ} + \overline{W}} + \overline{P} \overline{Q+ST}U + (N+R)(M+LOK) \\
H &= \overline{XYZ + ZXW} + \overline{PQU + STU} + NM + RM + NLOK + RLOK
\end{align*}
\]

2b. (5%) Compare the cost of the designs in 2a. and Problem 5 of homework 1 in terms of the number of transistors.

There are \(4\times6 + 4\times4 + 8\times4 = 72\) transistors with NAND gates.

There are 30 transistors for the compound gate implementation in homework 1. Clearly, the design with the compound gate can save area and is faster.
3. (10%) Sketch the side view (slice down into silicon) of a stacked contact that connects poly to metal4 using colored pens or pencils.

![Side view diagram]

4. (5%) List the steps needed to create the stacked contact that connects p+ diffusion to metal 3 using a positive photoresist process.

Deposit a positive photoresist on top of p- substrate
Apply a mask to mask away areas that the UV light can’t reach and expose etching the exposed photoresist and adding the donor atoms to create n-well remove the remaining photoresistance

NOTE: The above step was not part of what was asked for. Just included for completeness.

Deposit a positive photoresist on top of the n-well and p-substrate
Apply a mask to mask away areas that the UV light can’t reach and expose etch the exposed photoresist and add the p+ implants
remove the remaining photoresist

Deposit oxide on top of p+, n-well and the p- substrate
Deposit a positive photoresist on top of oxide
Apply a mask to mask away areas that the UV light can’t reach and expose etch the exposed photoresist
etch the oxide not under the photoresist to create cuts in the oxide remove the remaining photoresist

deposit metal 1
Deposit a positive photoresist on top of metal 1
Apply a mask to mask away areas that the UV light can’t reach and expose etch the exposed photoresist
etch the metal not under the photoresist. The remaining metal is the m1 contact to p+ remove the remaining photoresist

Deposit oxide on top of metal 1
Deposit a positive photoresist on top of oxide
Apply a mask to mask away areas that the UV light can’t reach and expose
etch the exposed photoresist
etch the oxide not under the photoresist to create cuts in the oxide
remove the remaining photoresist

deposit metal 2
Deposit a positive photoresist on top of metal 2
Apply a mask to mask away areas that the UV light can’t reach and expose
etch the exposed photoresist
etch the metal not under the photoresist. The remaining metal is the m2 contact to m1
remove the remaining photoresist

Deposit oxide on top of metal 2
Deposit a positive photoresist on top of oxide
Apply a mask to mask away areas that the UV light can’t reach and expose
etch the exposed photoresist
etch the oxide not under the photoresist to create cuts in the oxide
remove the remaining photoresist

deposit metal 3
Deposit a positive photoresist on top of metal 2
Apply a mask to mask away areas that the UV light can’t reach and expose
etch the exposed photoresist
etch the metal not under the photoresist. The remaining metal is the m3 contact to m2
remove the remaining photoresist

Note: There might be additional steps as sometimes the metal deposited in the contact cuts is not the same as the metal used for interconnections.

5. (5%) Sketch the crosssection of an NMOS transistor when $V_{ds}>V_{gs-Vt}$. Show clearly the shape of the channel.

![NMOS transistor diagram](image)

6. (5%) Explain what a channel stop is.
Channel stop is a technique used to avoid MOS parasitic transistors between two adjacent diffusions of the same type. It injects more p+ implants between two n+ diffusions to make it more difficult creating an accidental channel between these diffusions. To avoid pmos parasitic MOS transistors n+ implants are injected between two adjacent p+ diffusions.

7. (10%) In the figure below, draw the cross-section down into silicon along the horizontal yellow line.

![Cross-section diagram]

Note: the gray color is thick oxide

8a. (5%) In an inverter, if $V_{dd} = 1.8v$, and $V_{dsn} = 1v$, what is $V_{dsp}$?

$V_{dsp} = -0.8$ V

8b. (5%) If a PMOS transistor is used as a switch, with the gate voltage = 0.0v, if the $Vin = 0.0v$, and $V_{out} = 1.8v$, at $t=0+$, will the final output voltage be 0.0v?

The final voltage will not reach 0.0V because the source of the PMOS transistor is at the output. The source will decrease until it reaches $|V_{tp_{body-effect}}|$. 