1. Overview

In ee457, we learned how to design a simple 5 stage pipeline in great details. This pipeline corresponds to architectures designed at the beginning of the 1990’s. In ee557, we assume that these implementation details are known so that we can explore a large number of architectures at a more abstract level. We will learn about processors and systems as they are designed today. The focus of the course is not on research but on actual, commercial, existing machines. Towards the end of the class we will discuss some research issues. These issues are the topic of ee657.

2. Textbooks


3. Copies of transparencies : can be purchased from the USC bookstore.

3. Prerequisites:

1. CSCI455: Data Structures, C /Pascal programming
2. EE101: Digital Logic Design
3. EE357: Assembly Code Programming and Basic Machine Structure
4. EE457: Computer System Organization

4. Discussion session and Attendance:

EE-557 has two 75 minutes regular classes and a 50 minutes discussion session per week. The discussion session is an opportunity to discuss the material covered in class, the homework and the exams with the TA. At times class material may be expanded upon during the discussion session.

Although we will not check for presence either at regular class times or at the discussion session, I consider that attendance is mandatory. All material/information given out during regular class times and discussion session is part of the course. If you have to miss a class or a session, make sure that you catch up by asking a friend to brief you up. Also stay informed of homework deadlines, changes of deadlines, potential problems with homework questions etc. by visiting the web site regularly.

5. TA/Grader

1. TA: Spundun Bhatt. e-mail: bhatt@usc.edu. Office hours: M and W 2-3 in EEB201.
   Phone:(213)740-4336 (Call during office hours only.)
2. Grader: Kirit Lodhia. e-mail: lodhia@usc.edu. Office hours: M and Th 11-12 in EEB 201.
   Phone: (213)740-4336 (Call during office hours only.)

6. Course Content

1. Introduction, Motivation, Quantitative Aspects: PH Chapter 1.
2. Instruction Sets: PH Chapter 2.
4. Advance Processor Design (Superscalar, ILP, VLIW) PH Chapter 4.
5. Memory Hierarchy: PH Chapter 5.
9. Vector and SIMD Processing: PH Appendix B

7. Course Work:

1. Homework: There will be 5 or 6 homework. For on-campus students homework are due by 5pm in EEB 225, on the day of the deadline. Remote students must submit their homework to their TV coordinator on their site no later than 5pm on the date of the deadline. No late homework will be accepted.
2. Midterm #1: Date: Friday, October 5, during regular class time (second hour). Material: PH Chapters 1-3. Plus HP Chapters 1, 2, 3, 5, 6 and 7.
3. Midterm #2: Date: Friday, November 9, during regular class time (second hour). Material TBA.
4. Final: Date:
   Wednesday December 12, 11am-1pm
   All tests will take place on campus and all students must come to campus to take the tests.
   Please understand that there will be NO make-up exam, except in cases of personal medical emergency certified by a physician, or of personal accident. All other requests will be denied.

8. Grading Policy

   Homework: 10%; Midterm #1: 25%; Midterm #2: 25%; Final: 40%.

Please visit regularly the following class web site:

   For homework, exams, solutions, and news visit http://www-classes.usc.edu/engr/ee-s/557d/
   Also, visit the DEN site at DEN.usc.edu to access the webcast of each class. PLEASE note that the webcast of a class will be disabled after 2 weeks following the class. So you have two weeks to watch the webcast of a particular class.