Theory and Practical Implementation of Harmonic Resonant Rail Drivers

Joong-Seok Moon
William C. Athas*
Peter A. Beerel
University of Southern California
*Apple Computer Inc.
## Motivation

Low-power still growing in importance

Clock drivers and nodes remain largest power consumers

### Low-power VLSI techniques

- Clock gating
- Dynamic voltage supplies
- Asynchronous
- Resonant clock drivers
- Recycle energy of clock node

Our research focus
Classification of Resonant Clock Drivers

- **Sinusoids**
  - Easy and efficient to generate
  - Low overhead
  - Hard to work with, very “undigital”

- **Blips**
  - Advantages of sinusoids
  - Positive-bumps only

- **Harmonics (Quasi Square-Wave)**
  - Easy to work with, very “digital”
  - Design can be complex and costly
Prior Arts – Blips
(Athas et. al, ISCAS 1996)

+ All-resonant network
+ Yields almost non-overlapping two-phase clock
  - Balanced load capacitances required (not often available)
  - Frequency is sensitive to variations in clock loads $C_{L1}$, $C_{L2}$
Can be tuned for any shape, transition time, frequency

Requires multiple voltage supplies

Resulting frequency is sensitive to variation in clock load $C_L$

Prior Arts – Harmonics
(Younis and Knight, AVLSI 1996)
Proposed Harmonic Resonant Rail Driver

Background
- Current-Fed Pulse Forming Network (CPFN)

Design Algorithm
- Form linear system of equations to calculate needed component values

Implementation Issues

Lab Measurements

Conclusions
Background: Current-Fed Pulse Forming Network (CPFN)

Definition: Nth-order square-wave

\[ v(t) = \frac{2V_0}{\pi} \sin\frac{2\pi}{T} + \frac{2V_0}{3\pi} \sin\frac{6\pi}{T} + \frac{2V_0}{5\pi} \sin\frac{10\pi}{T} + \cdots + \frac{2V_0}{(2n-1)\pi} \sin\frac{2\pi(2n-1)t}{T} \]

Nth-order square-wave pulse generator
- Circuit template derived from definition

Issues
- Cascaded connection: no place for clock load
- Voltage swings negative (thus, need DC offset)
- Constant current source required
Background: Modified CPFN

Network Implementation:
- Same impedance/admittance function as original CPFN
- Provides location for clock load capacitance

Remaining Issues
- Voltage swings negative (thus, need DC offset)
- Constant current source required

New Issue
- More difficult to determine value of each component
Design Algorithm

Step 1: Convert to Frequency Domain

Given: N-th order square-wave equation

\[ v(t) = \frac{2V_0}{\pi} \sin \frac{2\pi}{T} t + \frac{2V_0}{3\pi} \sin \frac{6\pi}{T} t + \frac{2V_0}{5\pi} \sin \frac{10\pi}{T} t + \cdots + \frac{2V_0}{(2n-1)\pi} \sin \frac{2\pi(2n-1)t}{T} \]

Convert to frequency domain (Laplace transform)

\[ V(s) = \frac{2V_0\omega_0}{\pi} \left( \frac{1}{s^2 + \omega_0^2} + \cdots + \frac{1}{s^2 + (2n-1)^2 \omega_0^2} \right) \]

Identify all branch currents

\[ I_{CL}(s) = \frac{2V_0C_0\omega_0}{\pi} \left( \frac{s}{s^2 + \omega_0^2} + \cdots + \frac{s}{s^2 + (2n-1)^2 \omega_0^2} \right) \]

\[ I_{L0}(s) = \frac{2V_0\omega_0}{\pi L_0} \left( \frac{1}{s(s^2 + \omega_0^2)} + \cdots + \frac{1}{s(s^2 + (2n-1)^2 \omega_0^2)} \right) \]

\[ I_k(s) = \frac{1}{L_k} \frac{s}{s^2 + \frac{1}{L_k C_k}} \]

\[ V(s) = \frac{2V_0\omega_0}{\pi L_k} \frac{1}{s^2 + \Omega_k^2} \left( \frac{s}{s^2 + \omega_0^2} + \cdots + \frac{s}{s^2 + (2n-1)^2 \omega_0^2} \right) \quad \text{where} \quad \Omega_k = \frac{1}{\sqrt{L_k C_k}} \]
Design Algorithm
Step 2: Simplify $I_k(s)$

**Given**

$$I_k(s) = \frac{2V_0 \omega_0}{\pi L_k} \cdot \frac{1}{s^2 + \Omega_k^2} \left( \frac{s}{s^2 + \omega_0^2} + \cdots + \frac{s}{s^2 + (2n-1)^2 \omega_0^2} \right)$$

**Convert $I_k(s)$ using partial fraction expansion**

$$I_k(s) = \frac{2V_0 \omega_0}{\pi L_k} \left( \frac{A_{k_1}s}{s^2 + \Omega_k^2} + \frac{B_{k_1}s}{s^2 + \omega_0^2} + \cdots + \frac{A_{kn}s}{s^2 + \Omega_k^2} + \frac{B_{kn}s}{s^2 + (2n-1)^2 \omega_0^2} \right)$$

**By comparing each term,**

$$\frac{s}{(s^2 + \Omega_k^2)(s^2 + (2j-1)^2 \omega_0^2)} = \frac{A_{kj}s}{s^2 + \Omega_k^2} + \frac{B_{kj}s}{s^2 + (2j-1)^2 \omega_0^2}$$

$$s = (A_{kj} + B_{kj})s^3 + (A_{kj}(2j-1)\omega_0^2 + B_{kj} \Omega_k^2)s$$

$$A_{kj} + B_{kj} = 0$$

$$A_{kj}(2j-1)^2 \omega_0^2 + B_{kj} \Omega_k^2 = 1$$
Design Algorithm
Step 3: Find \( \Omega^2_k = 1/L_k C_k \)

Given

\[
I_k(s) = \frac{2V_0 \omega_0}{\pi L_k} \left( \frac{A_{k1}s}{s^2 + \Omega_k^2} + \frac{-A_{k1}s}{s^2 + \omega_0^2} + \cdots + \frac{A_{kn}s}{s^2 + \Omega_k^2} + \frac{-A_{kn}s}{s^2 + (2n-1)^2 \omega_0^2} \right)
\]

Rewrite for \( \Omega_k \)

\[
I_k(s) = \frac{2V_0 \omega_0}{\pi L_k} \left( \frac{(A_{k1} + A_{k2} + \cdots + A_{kn})s}{s^2 + \Omega_k^2} + \frac{-A_{k1}s}{s^2 + \omega_0^2} + \cdots + \frac{-A_{kn}s}{s^2 + (2n-1)^2 \omega_0^2} \right)
\]

By applying KCL, term with \( \Omega_k \) has to be zero

\[
\sum_{j=1}^{n} A_{kj} = 0
\]

Combining conditions yields characteristic equation

\[
A_{kj} ((2j-1)^2 \omega_0^2 - \Omega_k^2) = 1
\]

\[
A_{kj} = \frac{1}{(2j-1)^2 \omega_0^2 - \Omega_k^2}
\]

\[
\therefore \sum_{j=1}^{n} A_{kj} = \frac{1}{\omega_0^2} \sum_{j=1}^{n} \frac{1}{(2j-1)^2 - x} = 0, \quad \text{where} \quad x = \left( \frac{\Omega_k}{\omega_0} \right)^2
\]
Design Algorithm
Step 4: Substitute roots into KCL Equation

Given: n-1 roots from characteristic equation

\[ \Omega_1^2 = \alpha_1 \omega_0^2, \quad \Omega_2^2 = \alpha_2 \omega_0^2, \ldots, \quad \Omega_{n-1}^2 = \alpha_{n-1} \omega_0^2 \]

Coefficient \( A_{kj} \) is

\[ A_{kj} = \frac{1}{(2j-1)^2 \omega_0^2 - \Omega_k^2} = \frac{1}{\omega_0^2 (2j-1)^2 - \alpha_k} \]

We rewrite branch currents

\[
\begin{align*}
\frac{I_{DC}}{s} &- I_{C0}(s) = I_{L0}(s) + \sum_{k=1}^{n-1} I_k(s) \\
\frac{I_{DC}}{s} &- \frac{2C_0 V_0 \omega_0}{\pi} \left( \frac{s}{s^2 + \omega_0^2} + \cdots + \frac{s}{s^2 + (2n-1)^2 \omega_0^2} \right) \\
&= \frac{2V_0}{\pi L_0 \omega_0} \left( 1 + \frac{1}{3^2} + \cdots + \frac{1}{(2n-1)^2} \right) \frac{1}{s} \\
&- \frac{2V_0}{\pi \omega_0} \left( \frac{1}{L_0} + \frac{1}{L_1(1-\alpha_1)} + \cdots + \frac{1}{L_{n-1}(1-\alpha_{n-1})} \right) \frac{s}{s^2 + \omega_0^2} \\
&- \cdots \\
&- \frac{2V_0}{\pi \omega_0} \left( \frac{1}{(2n-1)^2 L_0} + \cdots + \frac{1}{L_{n-1}((2n-1)^2 - \alpha_{n-1})} \right) \frac{s}{s^2 + (2n-1)^2 \omega_0^2}
\end{align*}
\]
Design Algorithm

Step 5: Find $L_k$, $C_k$

By comparing both sides of current equation, find $L_k$

From $\Omega_k^2 = 1/L_kC_k$, find $C_k$
Implementation:
Issues with Modified CPFN

We found the recipe to identify all component values.

Still Remaining Issues
- Voltage swing: +V ~ -V
- Constant current source required
Implementation: Proposed Network

- Drive network using square-wave voltage source
  - Approximates Thevenin’s equivalent network
  - Introduces $V_{dc}/2$ DC offset

- Add large tank capacitance $C_T$ in series with $L_0$
  - Absorbs DC offset from input pulses

- Introduce series resistance $R$
  - Absorbs unwanted higher order harmonics
Implementation:
Frequency Response vs. R (1MHz, 2\textsuperscript{nd}-order)

\[ F(s) = \frac{V_o(s)}{V_i(s)} \]

- \(|F(s)| = 1, \ \text{phase}(F(s)) = 0\) at each harmonic frequencies
- Larger \(R\) absorbs higher order harmonics much better
Lab Measurement: Test Board Setup

- Measure current flowing into 74FCT244C CMOS buffer
- Capacitors and inductors are all tunable except tank capacitor $C_T$
- In conventional mode, $R$ is set to 0

<table>
<thead>
<tr>
<th></th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>S4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>2\textsuperscript{nd}-order</td>
<td>O</td>
<td>O</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3\textsuperscript{rd}-order</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>X</td>
</tr>
<tr>
<td>4\textsuperscript{th}-order</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
</tbody>
</table>
# Lab Measurement: Theoretical & Measured Component Value

<table>
<thead>
<tr>
<th>fclk MHz</th>
<th>C L</th>
<th>C1</th>
<th>L0</th>
<th>L1</th>
<th>R</th>
<th>P/fCV²</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Theory</td>
<td>Measured</td>
<td>Theory</td>
<td>Measured</td>
<td>Theory</td>
</tr>
<tr>
<td>2nd</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_H=3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_L=0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8</td>
<td>97.8</td>
<td>62.6</td>
<td>59.8</td>
<td>224.8</td>
<td>215.0</td>
<td>126.5</td>
</tr>
<tr>
<td>1.0</td>
<td>97.8</td>
<td>62.6</td>
<td>59.8</td>
<td>143.9</td>
<td>135.9</td>
<td>80.9</td>
</tr>
<tr>
<td>2.0</td>
<td>97.8</td>
<td>62.6</td>
<td>59.0</td>
<td>36.0</td>
<td>34.6</td>
<td>20.2</td>
</tr>
<tr>
<td>5.0</td>
<td>97.8</td>
<td>62.6</td>
<td>59.3</td>
<td>5.76</td>
<td>5.6</td>
<td>3.24</td>
</tr>
<tr>
<td>10.0</td>
<td>97.8</td>
<td>62.6</td>
<td>56.0</td>
<td>1.44</td>
<td>1.50</td>
<td>0.81</td>
</tr>
<tr>
<td>15.0</td>
<td>97.8</td>
<td>62.6</td>
<td>56.5</td>
<td>0.64</td>
<td>0.67</td>
<td>0.36</td>
</tr>
</tbody>
</table>

- Inductors and capacitors are tuned for minimal power consumption, then measured using LRC-meter.
- Measured values are within 10% of theoretical values.
Motivation
- How R affects power consumption and rise/fall time?

Experiment
- R: 100 ~ 2000 $\Omega$
- 2$^{nd}$-order, 1MHz, $C_L=100pF$

Result
- Rise/fall time decreases at the expense of power consumption
- Don’t have to design higher order network for fast rise/fall time
Lab Measurement: Varying $C_L$

Motivation
- In practice, load capacitance $C_L$ may vary from nominal value

Experiment
- $C_L$: Nominal 100pF (Varies +30% ~ -30%)
- 2$^{nd}$-order, 1MHz
- All other values are fixed

Result
- Output frequency is stable
- Normalized power consumption increases due to distortion
Lab Measurement: 1MHz, 2\textsuperscript{nd}-/3\textsuperscript{rd}-order Waveform

\begin{itemize}
  \item $f=1\text{MHz}$
  \item $C_L=100\text{pF}$
  \item 2\textsuperscript{nd}-order
  \item $R=2.015k\Omega$
  \item $P/fC^2=14.53\%$
  \item $f=1\text{MHz}$
  \item $C_L=100\text{pF}$
  \item 3\textsuperscript{rd}-order
  \item $R=1.671k\Omega$
  \item $P/fC^2=16.61\%$
\end{itemize}
Lab Measurement:
1MHz, 4\textsuperscript{th}-order/10MHz, 2\textsuperscript{nd}-order

\begin{align*}
\text{f}=1\text{MHz} \\
C_0=100\text{pF} \\
4\text{th}-\text{order} \\
R=0.958k \\
P/fCV^2=28.03\% \\
\end{align*}

\begin{align*}
\text{f}=10\text{MHz} \\
C_0=100\text{pF} \\
2\text{nd}-\text{order} \\
R=0.120k \\
P/fCV^2=19.58\% \\
\end{align*}
Conclusion

- Practical solution for harmonic resonant square-wave signal generator is proposed
- Proposed algorithm: Simple solution to determine (L, C) components’ values
- 70-85% energy efficiency measured in frequency ranges 0.8MHz~15MHz
  - Higher frequency range feasible
- Output frequency is relatively insensitive to load capacitance variation
- Can be applied to True Single Phase Clocking system without clock drivers (wide metal for clock node)