Lecture 14:

Introduction to Link Design

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Overview

Reading

Chapter 19 - High Speed Link Design, by Ken Yang, Stefanos Sidiropoulos

Introduction

There has been an explosion of interest in high-speed IO over the past 10 years. It is now being used in products ranging from DRAMs to interconnects in high-end servers and routers. This lecture will give an overview of the basic elements needed in a high-speed link, and will set up what we will discuss in the next few lectures. We start by looking at what makes driving external wires different from the work we have done driving internal wires.
Basic IO Design

All external signal paths can be represented by three elements:

Transmitter
• Converts bits to an analog electrical signal to transmit on pin

Channel
• Transmission media for the analog signal, which is sometimes pretty nasty to signal fidelity

Receiver
• Convert the analog signals back to bits (quantized in voltage and time)
• It is the need to convert back to digital signals that can be a problem
Basic Issues

**Voltage Margins**: making sure voltage quantization yields the correct result:

\[ \text{RxTx} \]

\[ R_{\text{TERM}} \]

\[ R_{\text{TERM}} \]

\[ \text{Channel} \]

\[ \text{Rx} \]

**Timing Margins**: knowing which bit is which:

\[
\begin{array}{cccccccc}
1 & 0 & 0 & 1 & 0 & 1 & 0 \\
\end{array}
\]

\[ \text{t}_{\text{bit}}/2 \]

- For a high-speed signal, bits are pretty short (< 1ns)
What is the Problem

Deal with analog signals all the time on chip. What is the issue with IO?
• Why are timing and voltage margins an issues for external signals?

The speed of light is not infinite
• Wire connecting the gates is not an equipotential
  - It is not even an RC line
• So life gets complicated
Finite Speed of Light

Signals on wires must experience delay in reaching destination -- $T_d = L/\nu$
- Bit arrive at a different time then when they were sent
- Must sample the data at the ‘correct’ time
- And the clocks to the two chips might not arrive at the same time

Wires store energy

- While the signal is travelling on the wire,
  - Current from Tx is initially set by the wire (can’t see resistor at $t=0$). $V/i$ for the line is its impedance, $Z$, and is set by the geometry of the wire
  - Signal is a pair of currents that propagates out from source (current and return)
Transmission Lines

(What wires are called when you notice \( v \) is not infinite)

Two constraints govern behavior at any junction:

- Voltage at all components must be equal
  Electrically connected
- Power flow into junction must equal power flow out of junction
  Conservation of energy
- Leads to reflections

\[
\frac{Z_2 - Z_1}{Z_1 + Z_2} \quad \text{and} \quad \frac{2Z_2}{Z_1 + Z_2}
\]

Signals can return to the source, as well as propagate forward

Note: the signal return path is usually drawn; it is as important as the signal
Conventional Buses

Have many problems
- Electrical distances from chip to chip vary, have stubs in the transmission lines
  - Make signal environment difficult
Stubs

Can’t connect to the middle of a transmission line without causing trouble:

Unless stub is short, it will cause reflections, since energy will split and only part will go into each transmission line segment:

- Add lots of ‘noise’ to the signal
- Slow the signal propagation
  - Energy must reflect off all the stubs before settling down
What Length is Short Enough?

Length is compared to distance light travels over what time?

- Related to the rise time of the signal, not frequency
  - If the signal does not change much by the time the reflection returns, you won’t see the reflection -- the reflection settles during the transition
  - If stub is short, energy storage in line is not significant
  - Model by lumped parameters

- Since fewer transmission lines are better, we want to slow signal edge rates
  - Bit should be 1/3 rise, 1/3 high, 1/3 fall
  - Risetime should be 1/2 to 2/3 of bit time

Nice edge rate for bits

Reflections are of small effective amplitude
Almost all high-speed links are point to point.

- Sending a clock as an additional data bit helps determine timing if the data cable lengths are all matched
- Called source synchronous links
Coupling

All transmission lines need a current return path

And are really differential systems

- Voltage difference between input and return is equal to the voltage difference between output and the voltage of the return at that end. The two return need not be at exactly the same voltage.

If return path is far away, another signal can ‘see’ the signal too

- Coupled transmission lines
  - $V_{out} = a \cdot V_{in1} + b \cdot V_{in2}$
- Coupling on PC board, and coax cables are small
- Coupling on Twisted pairs and IC packages is significant
Metrics

Need to measure links
• Look at a couple of metrics

Performance
• Bit rate
  - Normalize out the fabrication technology
    As technology scales, how fast will link become?
  - Use FO4
• Bit Error Rate (BER)
  - Link reliability
  - Signal to noise ratio
  - Should scale with technology, performance easy to predict
Bit Error Rate

Receiver needs to convert analog signal to digital value

• Possible to make an error -- noise is greater than signal
  - Voltage noise
  - Timing noise

  Reduces the amount of signal available

• BER
  - Depends on signal to noise ratio (SNR)
  - Also depends on noise statistics
BER and SNR

Many textbooks give plots like:

- Show BER exponentially related to SNR
- But assume gaussian noise
- Real noise is not gaussian
  - Small white (or colored noise) gaussian
  - Large self-induced noise
    
    Not true noise, but hard to calculate

Take true signal (signal - self-induced noise) and compare to white noise

- Give effective SNR
- White noise is small (mVs, but hard to estimate)
- Can make BER for most electronic links (non-optical) very, very small
Summary

Electronics need to deal with:

- Transmission line impedance
  - Need to have some method of dissipating the energy
  - Need to drive relatively low impedances (< 100 ohms)
- Noisy Signals
  - Some noise is proportional to signal amplitude
    Can’t perfectly set impedance or resistance, will have reflections
    Coupling of other signals
  - Fundamental noise in analog world
- Line Delay
  - Need to extract timing from signal or some other reference.