1. **IR Drop:** Design a power distribution network for a peripherally bonded ASIC. Your chip is 15*15 mm in area and contains 1M gate equivalents. Each gate equivalent drives a 200fF load (40fF of gate and 160 fF of wire) and switches on average every third cycle of a 100-MHz clock. What is the total power dissipation of your chip? Assuming a peak current to average current ratio of 4:1, what fraction of a metal layer (or how many metal layers) do you need to distribute power so that the overall supply fluctuation of a 2.5V supply is $\pm 250$ mV. Assume that the sheet resistance of the metal wires is 0.04 $\Omega$/square. Recall that average power dissipation of a gate is given by $P=0.5 C V^2 f \alpha$ where $C$ is its load capacitance, $V$ is the supply voltage level, $f$ is the clock frequency and $\alpha$ is its output activity factor.

2. **Capacitive Crosstalk:** Consider the circuit which is shown below:

<table>
<thead>
<tr>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{1a}$ (rise time)</td>
<td>100pS</td>
<td>$R_{1a}$</td>
<td>100 $\Omega$</td>
<td>$R_{1v}$</td>
<td>200 $\Omega$</td>
<td>$C_{1c}$</td>
</tr>
<tr>
<td>$V_{2a}$ (rise time)</td>
<td>150pS</td>
<td>$R_{2a}$</td>
<td>150 $\Omega$</td>
<td>$R_{2v}$</td>
<td>150 $\Omega$</td>
<td>$C_{2c}$</td>
</tr>
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<td>$V_{3a}$ (rise time)</td>
<td>200pS</td>
<td>$R_{3a}$</td>
<td>200 $\Omega$</td>
<td>$R_{3v}$</td>
<td>100 $\Omega$</td>
<td>$C_{3c}$</td>
</tr>
</tbody>
</table>
a. Find the maximum noise of nodes N1, N2, and N3 according to Devgan’s method
b. Find the maximum noise of nodes N1, N2, and N3 according to Vittal’s method
c. Find the maximum noise of nodes N1, N2, and N3 according to Hspice simulation (attach the voltage waveforms)

3. **Capacitive Cross Talk and Delay:** you are designing a chip that has a 2mm long data bus of 0.6μm wires on 1.2μm centers (see following figure) Assume the capacitance numbers from the table “On-chip Parasitic Capacitance” in Appendix II of chapter 3 handout and assume that the perpendicular wires on adjacent layers are all grounded. You are driving each bus line with a static driver that can accurately be modeled as a voltage source in series with a 1KΩ resistor. Assuming that all lines switch simultaneity to random states, what is the worst-case maximum and minimum delay of a line. (give an RC time constant)? (Hint: what combinations of transactions on adjacent lines will speed up or slow down a transition on a given bit?)

![Diagram of wires](image)

4. **Transmission Lines Cross Talk:** your printed-circuit layout contractor has inadvertently run a full-swing (3.3V) CMOS signal with a fast 500pS rise time right next to a slow swing (300mV) signal for a 10cm run of microstrip line. The lines are each 8 mils wide spaced 6 mils above a ground plane and spaced 8 mils from one another, a geometry that matches the first line of the table “Typical Transmission Line Parameters and Coupling Coefficients” in Appendix II of chapter 3 handout. Both lines are parallel terminated at the receiving end only. What is the magnitude of the noise induced on the low-swing line? Is this a concern?

5. **Signal-Return Cross Talk:** you have an integrated circuit package that can be accurately modeled as a lumped 5nH inductor for each pin. You plan to use this package to house a chip that drives 128 full-swing (3.3V) outputs into 50Ω lines with 1nS rise times. How many return pins do you need if the drop across the returns must be kept less than 300mV in the worst case? How many returns are needed if the rise time is slowed to 3nS?

6. **Skin Effect:** Show that the high frequency resistance of a coaxial cable is

\[ R = \frac{1}{2} \sqrt{\frac{\rho \mu f}{\pi}} \left( \frac{1}{r_1} + \frac{1}{r_2} \right) \]

where \( r_1 \) and \( r_2 \) are the radii of the inner and outer conductors, respectively. Further, show that the losses due to the skin effect are minimized for a particular value of the ratio \( r_1/r_2 \)