1. Consider an inverter with \( \frac{W_p}{W_n} = \frac{50\lambda}{25\lambda} \) in 0.18 \( \mu \) technology driving a load \( C_L \) thru ideal wires.
   a) Generate a two-dimensional look up table for reading off the 50\% input-to-output propagation delay and falling output transition time for the inverter. Use four values for the rising input transition time from 50 to 200 ps (in steps of 50 ps) and four values for load capacitance from 100 to 400 fF (in steps of 100 fF).
   b) Use the four term k-factor approximation and the linear interpolation equations to calculate the propagation delay and falling output transition time for a rising input transition time of 120 ps and load capacitance of 245 fF.
   c) Compare interpolation-based prediction of part b with actual hspice simulation.

2. Consider the two circuits depicted below.

   a) Do HSpice simulations and find the effective capacitance for the above two circuits by simulation.
   b) Use the table lookup from Problem 1 along with Macy’s approach to calculate the effective capacitance for each case. You must terminate the iteration loop so as to achieve gate delay estimates with a precision of three decimal points.
   c) Comment on the accuracy of the Macy’s approach compared to HSpice simulations.

   \[
   \gamma = 0.9997 - 3.7905\beta + 45.8006\beta^2 - 0.1605\alpha + 17.3641\alpha\beta - 183.8401\alpha\beta^2
   \]

Hint: use following equation instead of Macy’s diagram. All coefficients in the following equation obtained according to these metrics:
For Capacitances: \( fF \) (femto Farad)
For Output Transition Time (Tout which is 10\% t 90\% of output transition time): \( pS \) (pico Second)
For Resistance: Ohm (\( \Omega \))
3. Do HSpice simulation for the inverter of Problem 1 driving a 1 cm of on-chip transmission line terminated with a capacitive load of 800 fF. Plot the output waveform at the near-end and the far-end of the line. What behavior do you observe: lossless LC or lossy RC? Justify your answer.
Hint: for the transmission line you can use add following statements to you hspice file:

```
W1 near_end 0 far_end 0 N=1 L=0.01 RLGCMODEL=problem1_3
.Model problem1_3 W MODELTYPE=RLGC N=1
+Lo=1923nH
+Co=246584fF
+Ro=16666.6
```

4. For the circuit shown:
   a) Find the input admittance function Y(s) looking into node A.
   b) Find the first four moments of the input admittance function.

<table>
<thead>
<tr>
<th>Value</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_1 100 Ω</td>
<td>C_1 25 fF</td>
<td>L_1 1 nH</td>
</tr>
<tr>
<td>R_2 150 Ω</td>
<td>C_2 50 fF</td>
<td>L_2 2 nH</td>
</tr>
<tr>
<td>R_3 200 Ω</td>
<td>C_3 75 fF</td>
<td>L_3 1 nH</td>
</tr>
<tr>
<td>** ****</td>
<td>C_4 50 fF</td>
<td>** ****</td>
</tr>
</tbody>
</table>

5. Consider again the circuit of Problem 4. This time assume that all inductances are zero.
   a) Find the voltage transfer function from node A to node D.
   b) Find the first and second moments of the above transfer function using Taylor expansion.
   c) Find the Elmore delay and S2P delay of the circuit from node A to node D.
   d) Do HSpice simulations and find the delay. Which of the two delays is more accurate?
   e) Where does Elmore delay give provide a good estimation? Why?